1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
02		421247	ENGINEERING RELEASED	01/19/06	?

SCHEM,SYMPHONY,M9
EVT
1/19/06

PDF PAGE	CSA PAGE	CONTENTS	SYNC MASTER	DATE
1	1	Table of Contents	N/A	N/A
2	2	Block Diagram	SIREN	01/06/2006
3	4	BOM CONFIGURATION	(MASTER)	(MASTER)
4	6	Aliases	SIREN	01/06/2006
5	51	Left USB Port	SIREN	01/06/2006
6	53	ExpressCard Connector	SIREN	01/06/2006
7	54	PCI-E MiniCard Connector	SIREN	01/06/2006
8	55	MLB I/O Board Connector	SIREN	01/06/2006
9	64	Left ALS	SIREN	01/06/2006
10	68	AUDIO: CODEC	AUDIO_M9_PRO_LIO	01/06/2006
11	70	AUDIO: LINE IN	AUDIO_M9_PRO_LIO	01/06/2006
12	71	AUDIO: HEADPHONE AMP	AUDIO_M9_PRO_LIO	01/06/2006
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14	73	AUDIO: JACKS	AUDIO_M9_PRO_LIO	01/19/2006
15	74	AUDIO: JACK TRANSLATORS	AUDIO_M9_PRO_LIO	01/06/2006
16	78	3.3V Supply	SIREN	01/06/2006
17	82	DC-In & Battery Connectors	SIREN	01/06/2006
18	84	LEFT I/O POWER CONNECTOR	SIREN	01/06/2006
19	85	Cross Reference Page		
20	86	Cross Reference Page		
21	87	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7066	1	SCHEM,SYMPHONY,NEW,M9	SCH1	
820-1970	1	PCBF,SYMPHONY,M9	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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TITLE
SCHEM,SYMPHONY,NEW,M9

DRAWING NUMBER 051-7066 REV. 02

SHT 1 OF 87

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J8215
PBus/Battery Power Connector

18V5_DCIN

PP5V_S5_LIO

5V_S0_AUDIO_PWR

J8200
DC-In Jack

18V5_DCIN

3V42_G3H

U8200

AC Adapter Detect

U7800

3.3V S3/S0 Supply

3V3_S0

3V3_S3

J5110
Left USB Port2

U5100

J5100
Left USB Port1

USB Pwr Controller

J5500
LIO-MLB Flex Connector

PBUS

DCIN_G3H

3V42_G3H

U5300

3V3_S0

3V3_S3

ExCard Pwr Switcher

J5300
PCI-ExpressCard 34 Connector

VR6800

5V_S0_AUDIO

Audio 4.5V Supply

3V3_S0

1V5_S0

J7350
Audio In/SPDIF Rx Jack

U6800

J7380
Mic Connector

Audio Codec

J5400
PCI-E miniCard (Airport) Connector

3V3_S0

3V3_S3

5V_S0_AUDIO_PWR

J7300
Audio Out/SPDIF Tx Jack

U7210

U6401

J7382
Speaker Connector

Speaker Amp

U7230

Speaker Amp

LEFT ALS

U7240

J7381
Speaker Connector

U7220

Speaker Amp

Block Diagram

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE	SHT	OF
NONE	2	87

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BOM NUMBER	BOM NAME	BOM OPTIONS
630-7510	PCBA,SYMPHONY,NEW,M9	075-0199,075-0200
075-0200	PROJ_PTS,SYMPHONY,NEW,M9	COMMON,EXCARD_3CNTL,ONEWIRE_DIV,ONEWIRE_PWRCTL
075-0199	LEMENU_PTS,SYMPHONY,NEW,M9	LEMENU

PHANTOM BOM #'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0200	1	PROJ PTS,SYMPHONY,M9	BOM1		075-0200
075-0199	1	LEMENU PTS,SYMPHONY,M9	BOM2		075-0199

BAR CODE LABEL / EEE#'S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
000-0041	1	PLACEHOLDER FOR EEE/CCC INFO	[EEE:V3P]	CRITICAL	

BOM CONFIGURATION

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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D	051-7066	02

SCALE NONE SHT 4 OF 87

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POWER & GROUNDS

8 =PPBUS_G3H_LIO_CONN → PPBUS_G3H_LIO_CONN =PPVIN_S3_3V3S3 16
MAKE_BASE=TRUE
VOLTAGE=18.5V
MIN_LINE_WIDTH=1mm
MIN_NECK_WIDTH=0.25mm

8 =PP1V5_S0_LIO → PP1V5_S0_LIO
MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.20mm
=PP1V5_S0_MINI 7
=PP1V5_S0_EXCARD 6

16 =PP3V3_S3_REG → PP3V3_S3_LIO
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
=PP3V3_S3_MINI 7
=PP3V3_S3_EXCARD 6
=PP3V3_S3_LFTALS 9

16 =PP3V3_S0_FET → PP3V3_S0_LIO
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
=PP3V3_S0_MINI 7
=PP3V3_S0_AUDIO 10 14 15
=PP3V3_S0_EXCARD 6

18 =PP5V_S5_LIO → PP5V_S5_LIO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
=PP5V_S5_LTUSB 5
=PP5V_S5_3V3S3 16

13 12 10 8 =PP5V_S0_AUDIO → PP5V_S0_AUDIO_LIO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM

18 13 =PP5V_S0_AUDIO_PWR → PP5V_S0_AUDIO_PWR_LIO
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.20 MM

18 14 13 =GND_AUDIO_PWR → GND_AUDIO_PWR
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
GND_AUDIO
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.2MM

8 =GND_AUDIO → =GND_AUDIO_CODEC 10 11 12 13 14 15

CHASSIS_GND1
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
=GND_CHASSIS_LTUSB 5
=GND_CHASSIS_DCIN_JACK 17

CHASSIS_GND2
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
=GND_CHASSIS_AUDIO_JACK 14
=GND_CHASSIS_AUDIO_MIC 15

CHASSIS_GND3
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
=GND_CHASSIS_AUDIO_SPKRCONN 14

CHASSIS_GND4
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm
=GND_CHASSIS_LIO_FLEX 8
=GND_CHASSIS_PCIE_EXCARD 6

GND
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm

PCI-E EXPRESS CARD 34

8 =USB2_EXCARD_P → USB2_EXCARD_P 6
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

8 =USB2_EXCARD_N → USB2_EXCARD_N 6
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

8 =PCIE_CLK100M_EXCARD_P → PCIE_CLK100M_EXCARD_P 6
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_CLK100M_EXCARD_N → PCIE_CLK100M_EXCARD_N 6
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_EXCARD_D2R_P → PCIE_EXCARD_D2R_P 6
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_EXCARD_D2R_N → PCIE_EXCARD_D2R_N 6
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_EXCARD_R2D_P → PCIE_EXCARD_R2D_P 6
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_EXCARD_R2D_N → PCIE_EXCARD_R2D_N 6
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =EXCARD_CLKREQ_L → EXCARD_CLKREQ_L 6
MAKE_BASE=TRUE

8 =EXCARD_OC_L → EXCARD_OC_L 6
MAKE_BASE=TRUE

8 PCIE_WAKE_L → PCIE_WAKE_EXCARD_L 6
MAKE_BASE=TRUE PCIE_WAKE_MINI_L 7

7 6 PLT_RESET_L → LIO_PLT_RESET_L 8
MAKE_BASE=TRUE

16 8 =LIO_P3V3S3_EN → LIO_P3V3S3_EN =USB_LEFT_PWRON 5
MAKE_BASE=TRUE

PCI-E MINICARD

8 =PCIE_MINI_R2D_P → PCIE_MINI_R2D_P 7
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_MINI_R2D_N → PCIE_MINI_R2D_N 7
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_MINI_D2R_P → PCIE_MINI_D2R_P 7
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_MINI_D2R_N → PCIE_MINI_D2R_N 7
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_CLK100M_MINI_P → PCIE_CLK100M_MINI_P 7
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

8 =PCIE_CLK100M_MINI_N → PCIE_CLK100M_MINI_N 7
MAKE_BASE=TRUE NET_SPACING_TYPE=PCIE NET_PHYSICAL_TYPE=PCIE

7 USB2_MINI_P → TP_USB2_MINI_P
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

7 USB2_MINI_N → TP_USB2_MINI_N
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

8 =MINI_CLKREQ_L → MINI_CLKREQ_L 7
MAKE_BASE=TRUE

USB

5 USB_LEFT_P → =USB2_LT_P 8
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

5 USB_LEFT_N → =USB2_LT_N 8
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

5 USB_LEFT_OC_L → =LTUSB_OC_L 8
MAKE_BASE=TRUE

5 USB_LEFT2_P → =USB2_LT2_P 8
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

5 USB_LEFT2_N → =USB2_LT2_N 8
MAKE_BASE=TRUE NET_SPACING_TYPE=USB NET_PHYSICAL_TYPE=USB

5 USB_LEFT2_OC_L → =LT2USB_OC_L 8
MAKE_BASE=TRUE

SMBUS

8 =SMBUS_SB_SDA → SMBUS_SB_SDA 8
MAKE_BASE=TRUE
=SMBUS_EXCARD_SDA 6

R0600
0
1 2 SMBUS_MINI_SDA =SMBUS_MINI_SDA 7
MAKE_BASE=TRUE
5% 1/16W MF-LF 402

8 =SMBUS_SB_SCL → SMBUS_SB_SCL 8
MAKE_BASE=TRUE
=SMBUS_EXCARD_SCL 6

R0601
0
1 2 SMBUS_MINI_SCL =SMBUS_MINI_SCL 7
MAKE_BASE=TRUE
5% 1/16W MF-LF 402

Aliases

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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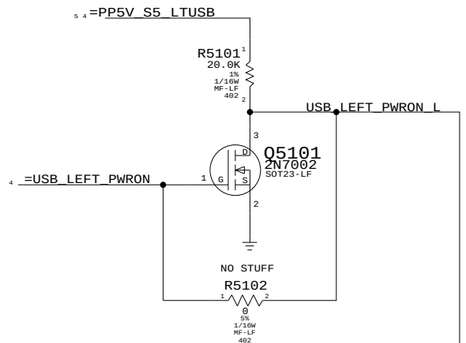
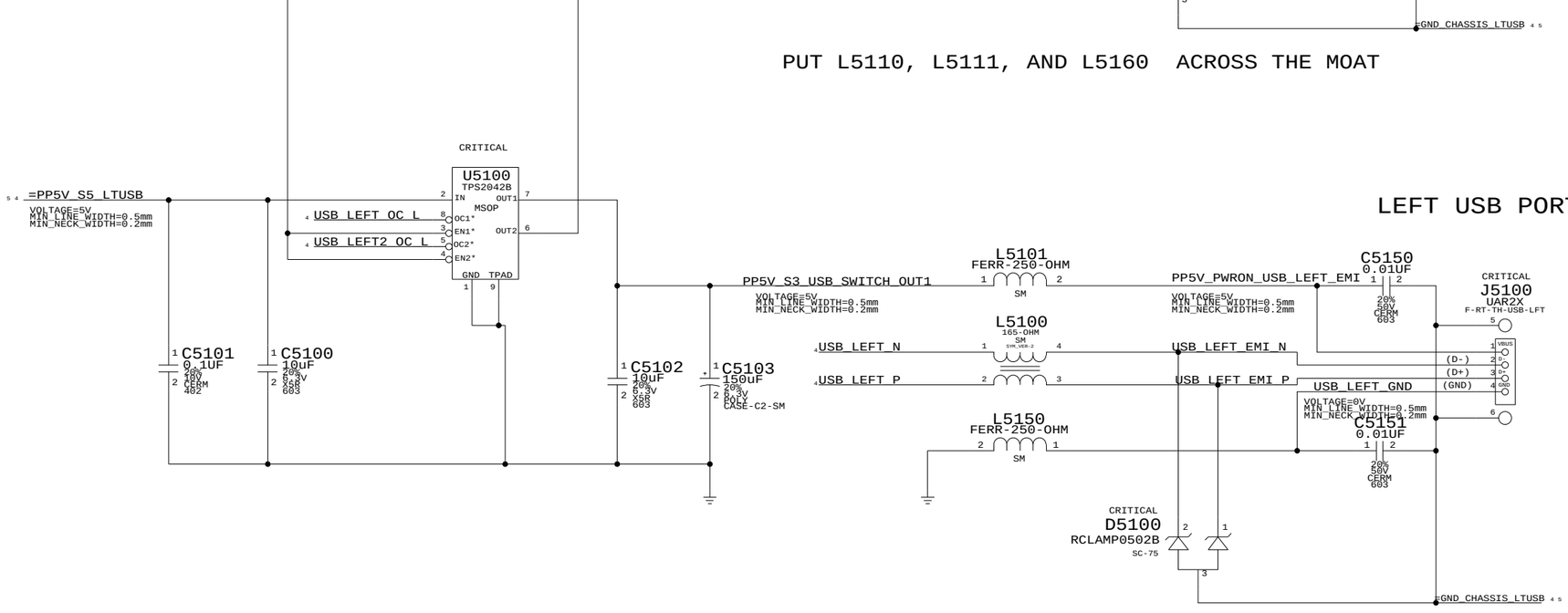


Stuff R5102 if TPS2052B so EN is high.



PUT L5100, L5101, AND L5150 ACROSS THE MOAT

PUT L5110, L5111, AND L5160 ACROSS THE MOAT

Left USB Port

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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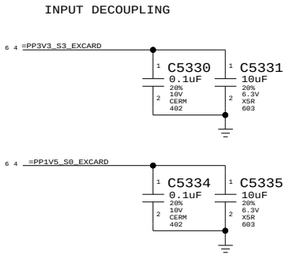
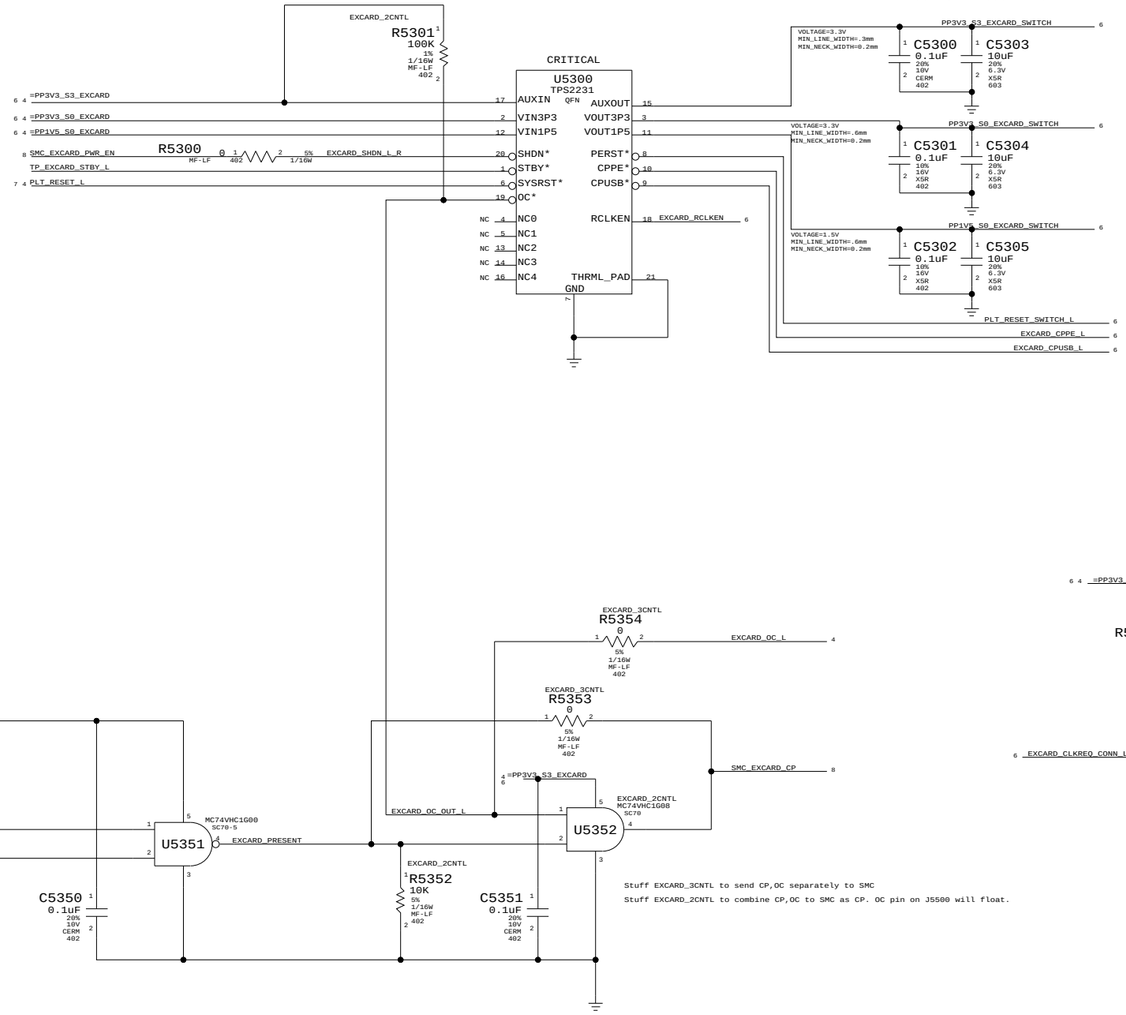
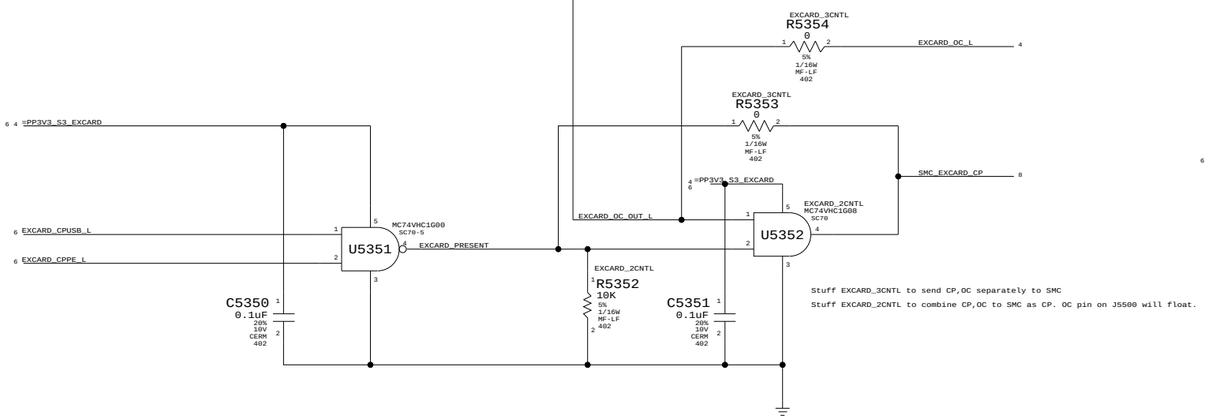
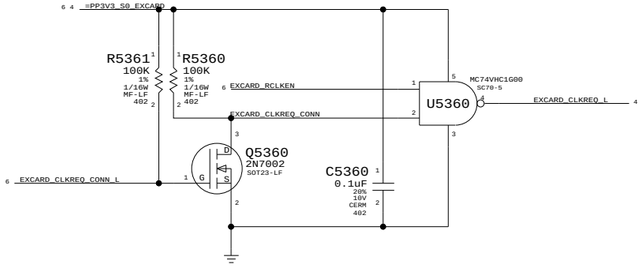
PCI-EXPRESS CARD 34 TOP MOUNT CONNECTOR


INPUT DECOUPLING
=PP3V3_S3_EXCARD
C5330 0.1uF 20% 10V CERM 402
C5331 10uF 20% 6.3V X5R 603
=PP1V5_S0_EXCARD
C5334 0.1uF 20% 10V CERM 402
C5335 10uF 20% 6.3V X5R 603







ExpressCard Connector

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SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE: NONE SHT 53 OF 87

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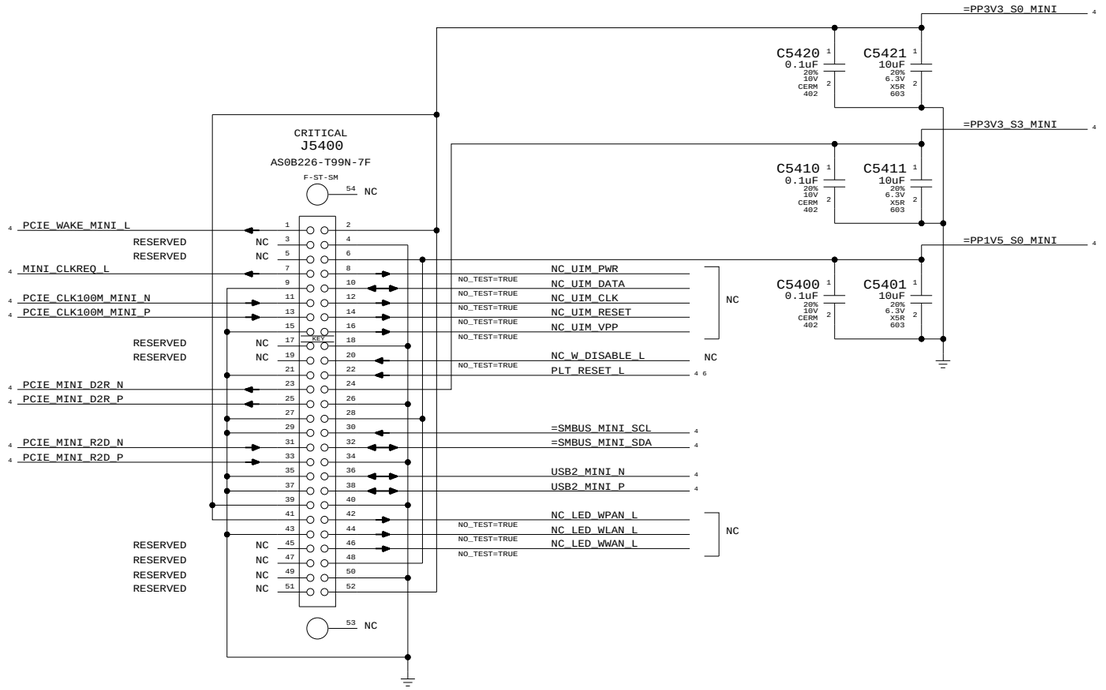
PCI-EXPRESS MINI CARD CONNECTOR



PCI-E MiniCard Connector

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE: NONE SHT 54 OF 87

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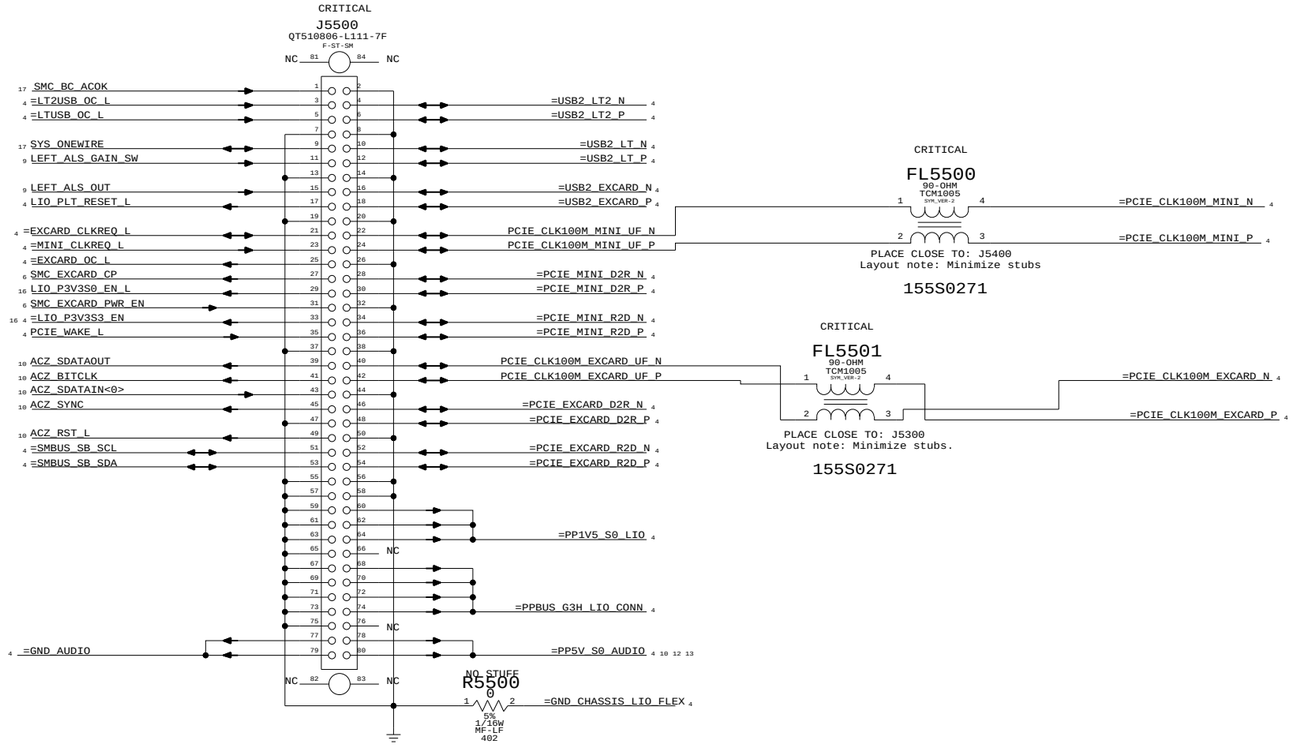
Left I/O Board Connector



MLB I/O Board Connector

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE	SHT
NONE	55 OF 87

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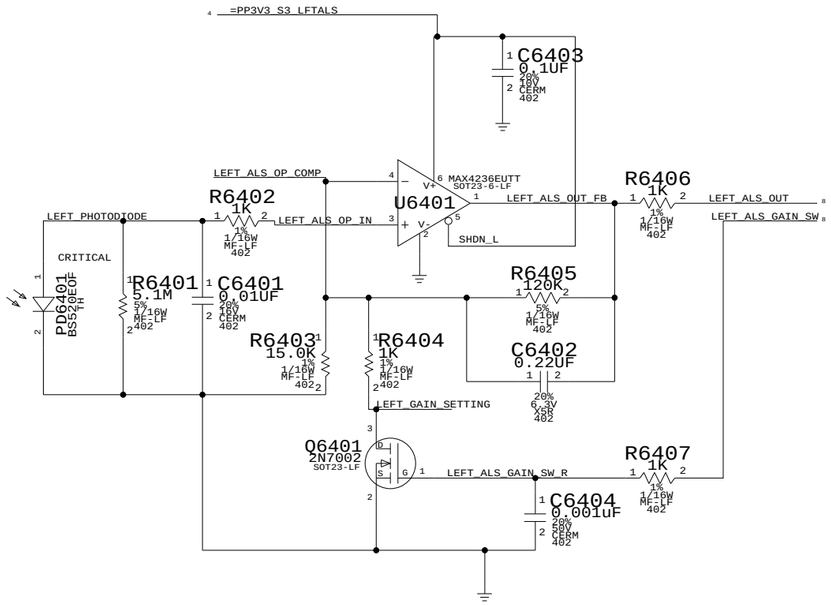

Left ALS

SYNC_MASTER=SIREN

SYNC_DATE=01/06/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE	SHT
NONE	64 OF 87

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AUDIO CODEC

APPLE P/N 353S1345

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
=PP3V3_S0_AUDIO

L6801
FERR-120-OHM-1.5A
0402

CRITICAL C6800 10UF 20% 6.3V X5R 603
CRITICAL C6801 0.001uF 10% 50V CERM 402
CRITICAL C6835 0.001uF 10% 50V CERM 402

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
PP3V3_AUDIO_CODEC

L6802
FERR-120-OHM-1.5A
0402

L6803
FERR-120-OHM-1.5A
0402

PP4V5_AUDIO_ANALOG
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=4.5V

VOLTAGE=4.5V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
PP4V5_AUDIO_ANALOG_FI

PP4V5_AUDIO_ANALOG_F
VOLTAGE=4.5V
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM

CRITICAL C6802 10UF 20% 6.3V X5R 603
CRITICAL C6830 0.001uF 10% 50V CERM 402
CRITICAL C6826 10UF 20% 6.3V X5R 603
CRITICAL C6836 0.001uF 10% 50V CERM 402

=GND_AUDIO_CODEC

PLACE NEAR U6800

R6808 22 5% 1/16W MF-LF 402

GND_AUDIO_DGND
ACZ_BITCLK
ACZ_SYNC
ACZ_SDATAOUT
ACZ_SDATAIN<0>
R6807 39 5% 1/16W MF-LF 402
SDATAIN
NC_AUD_GPIO_2
AUD_GPIO_0_R
AUD_GPIO_1_R
AUD_BI_PORT_C_L
AUD_BI_PORT_C_R
AUD_BI_PORT_D_L
AUD_BI_PORT_D_R
BAL_IN_L
BAL_IN_COM
BAL_IN_R
NC_VOL_UP
NC_VOL_DOWN
BEEP
ACZ_RST_L

LEMENU
U6800
STAC9220
LQFP

DVDD_CORE1	1		
DVDD_CORE3	9		
AVDD1	25		
AVDD2	38		
BIT_CLK	6		
SYNC	10		
SDATA_OUT	5		
SDATA_IN	8		
GPIO2	44		
GPIO0	45		
GPIO1	46		
PORT-C_L	23		
PORT-C_R	24		
PORT-D_L_HP	35		
PORT-D_R_HP	36		
CD-L	18		
CD-G	19		
CD-R	20		
VOLUME_UP	2		
VOLUME_DOWN	3		
PC_BEEP	12		
RESET*	11		
DVSS3	7		
DVSS2	4		
AVSS1	26		
AVSS3	42		
SPDIF-OUT	48	AUD_SPDIF_OUT_R	AUD_SPDIF_OUT
GPIO3/SPDIFIN	47		AUD_SPDIF_IN
SENSE_A	13		AUD_SENSE_A
SENSE_B	34		AUD_SENSE_B
HP PORT-A_L_HP	39		AUD_BI_PORT_A_L
HP PORT-A_R_HP	41		AUD_BI_PORT_A_R
LO PORT-F_L_HP	16		AUD_BI_PORT_F_L
LO PORT-F_R_HP	17		AUD_BI_PORT_F_R
VREFOUT-A	37	NC	
MIC1 PORT-E_L	14		AUD_BI_PORT_E_L
MIC1 PORT-E_R	15		AUD_BI_PORT_E_R
VREFOUT-B	28		
MIC2 PORT-B_L	21		AUD_BI_PORT_B_L
MIC2 PORT-B_R	22		AUD_BI_PORT_B_R
VREFOUT-C	29		AUD_VREF_PORT_C
VREFOUT-D	32	NC	
VREF_FILT	27	AUD_VREF_FILT	AUD_VREF_PORT_B
AFILT1	30	AUD_ANALOG_FILT_1	
AFILT2	31	AUD_ANALOG_FILT_2	
CAP2	33	AUD_BYPASS	
NC1	40	NC	
NC2	43	NC	

R6800 100K 5% 1/16W MF-LF 402
CRITICAL C6821 0.1UF 10% 16V X5R 402
XW6801 SM
=GND_AUDIO_CODEC
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

CRITICAL C6804 10uF 20% 6.3V TANT SMA-LF
CRITICAL C6812 0.001uF 10% 50V CERM 402
CRITICAL C6805 1000PF 5% 25V CERM 603
CRITICAL C6806 1000PF 5% 25V CERM 603
CRITICAL C6807 10UF 20% 6.3V TANT SMA-LF
CRITICAL C6813 0.001uF 10% 50V CERM 402

CRITICAL C6809 10uF 20% 6.3V TANT SMA-LF
CRITICAL C6832 0.001uF 10% 50V CERM 402
CRITICAL C6810 10uF 20% 6.3V TANT SMA-LF
CRITICAL C6833 0.001uF 10% 50V CERM 402

R6852 0 5% 1/16W MF-LF 402
AUD_GPIO_0 → AUD_GPIO_0_R

R6853 0 5% 1/16W MF-LF 402
AUD_GPIO_1 → AUD_GPIO_1_R

AUDIO DIGITAL GROUND ISOLATION

XW6800 SM
GND_AUDIO_DGND
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

4.5V POWER SUPPLY FOR CODEC

NO STUFF
D6800
POWERDI-123
DFLS140
CRITICAL

MIN_LINE_WIDTH=0.60 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
=PP5V_S0_AUDIO

L6800
FERR-120-OHM-1.5A
0402

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V
5V_REG_IN

VR6800
TPS79501
SOT223-6
IN
EN
OUT
NR/FB
GND
TAB

AUD_4V5_SHDN_L

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=4.5V
PP4V5_AUDIO_ANALOG

R6802 1K 1% 1/16W MF-LF 402
=PP3V3_S0_AUDIO

CRITICAL C6823 0.1UF 10% 16V X5R 402
CRITICAL C6822 10UF 20% 6.3V X5R 603

R6810 78.7K 1% 1/16W MF-LF 402
VREG_FB
CRITICAL C6825 15PF 5% 50V CERM 402
R6811 29.4K 1% 1/16W MF-LF 402
CRITICAL C6803 100UF 20% 6.3V POLY B2

=GND_AUDIO_CODEC
NO STUFF
R6803 0 5% 1/16W MF-LF 402
GND_AUDIO_DGND

APN: 353S1233

AUDIO: CODEC

SYNC_MASTER=AUDIO_M9_PRO_LIO
SYNC_DATE=01/06/2006

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D	051-7066	02
SCALE: NONE	SHT 68 OF 87	

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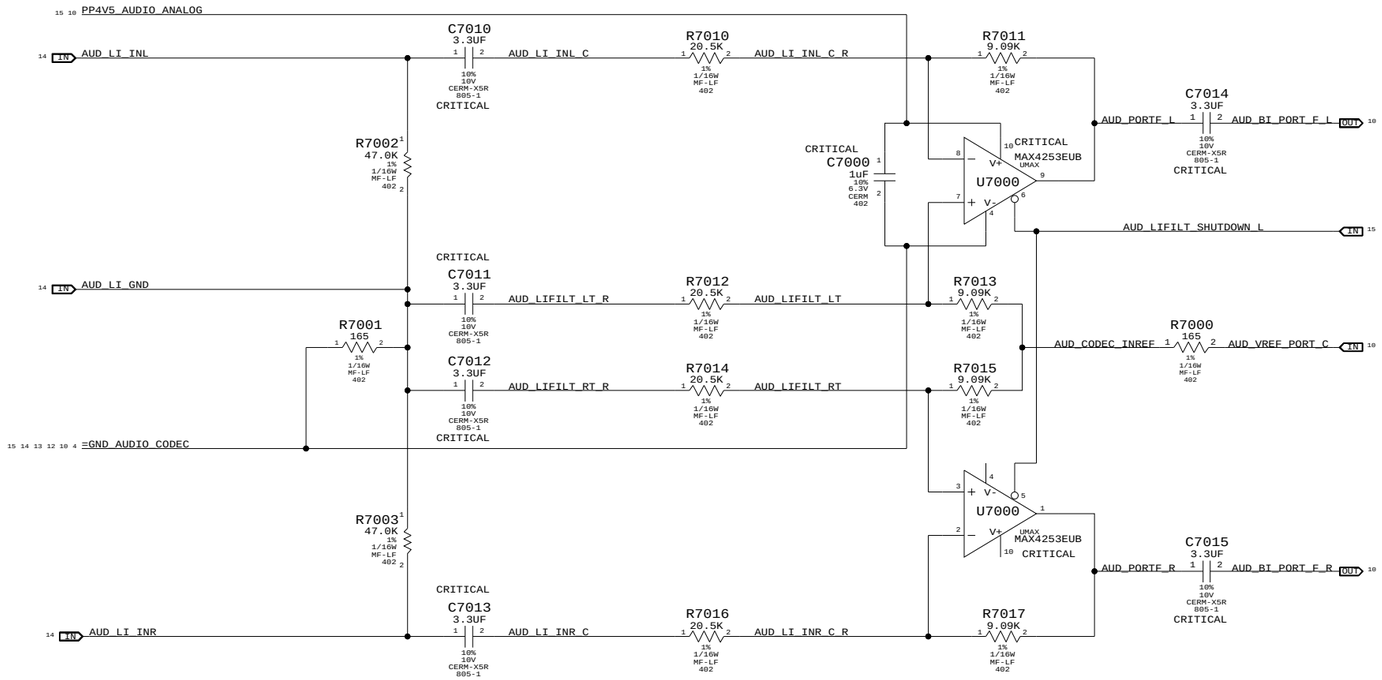
Pseudo-Diff Line-In Filter
GAIN = -7.1DB AV = 0.44
FC = 2.4 HZ



AUDIO: LINE IN

SYNC_MASTER=AUDIO_M9_PRO_LIO SYNC_DATE=01/06/2006

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SCALE: NONE	SHT 70 OF 87	

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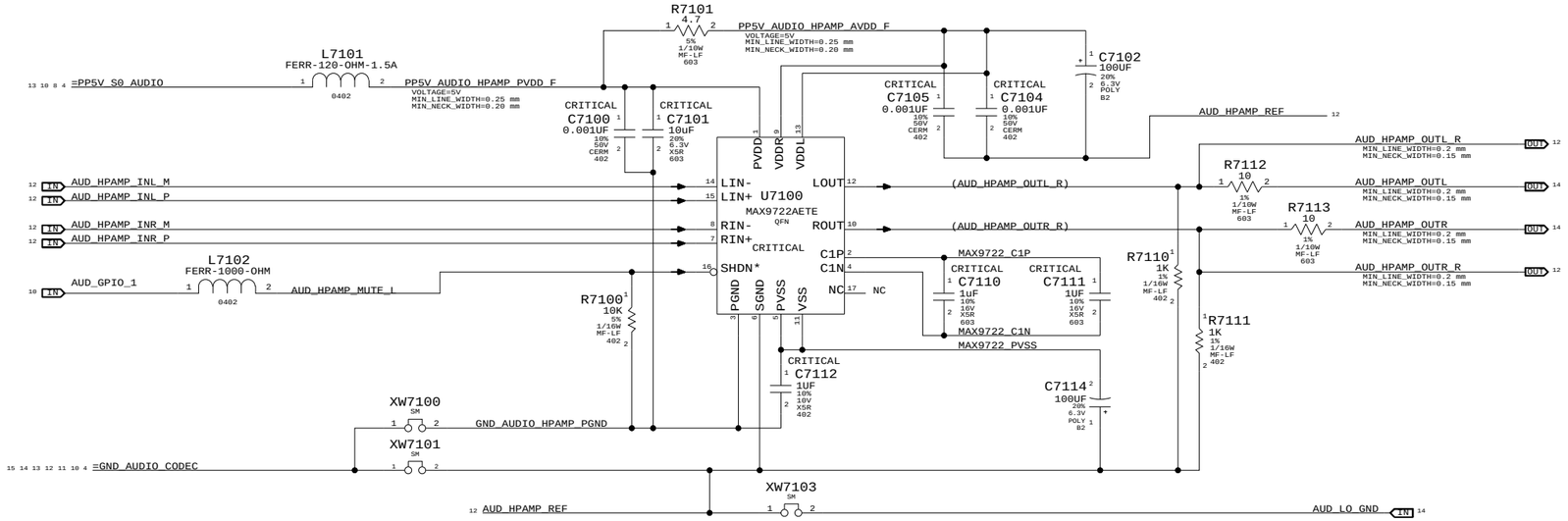
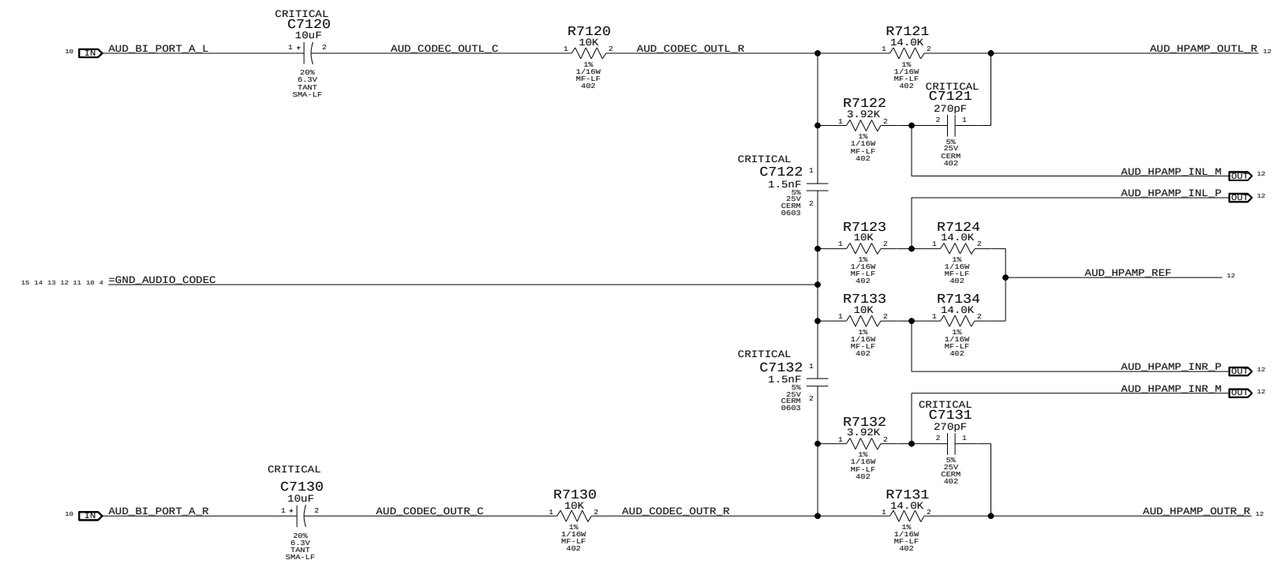
Headphone Amplifier (MAX9722)
APN:353S0959
VOLTAGE GAIN:1.4



2nd Order DAC Filter
HP:1.6 HZ



AUDIO: HEADPHONE AMP

SYNC_MASTER=AUDIO_M9_PRO_LIO SYNC_DATE=01/06/2006

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D	051-7066	02

SCALE	SHT
NONE	71 OF 87

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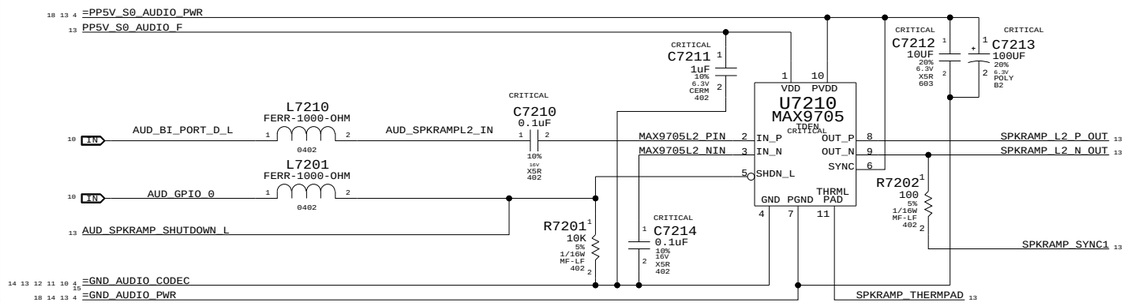
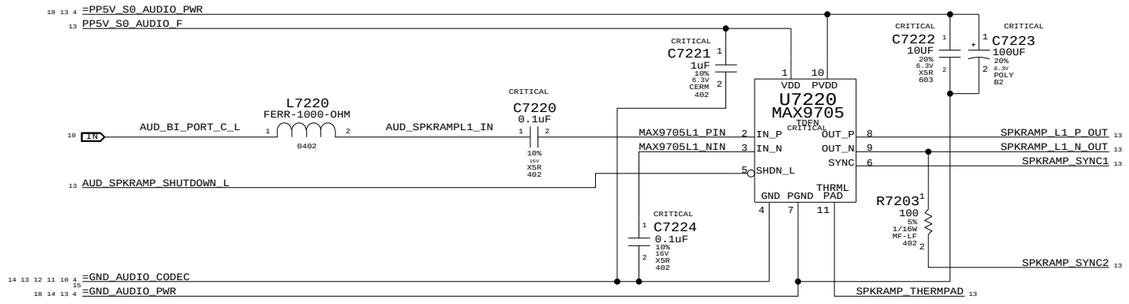
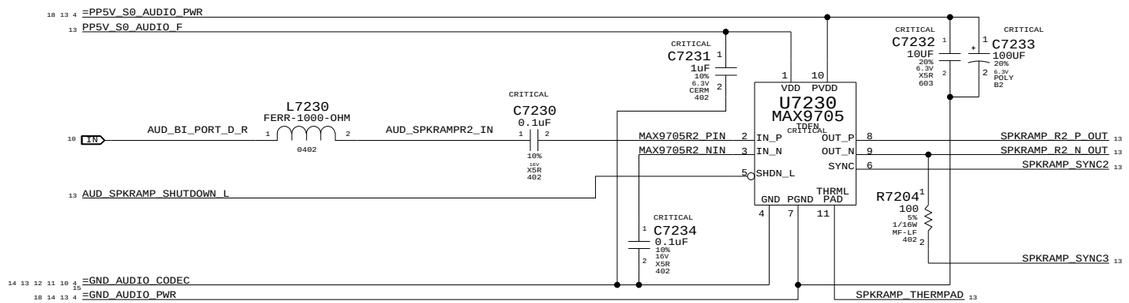
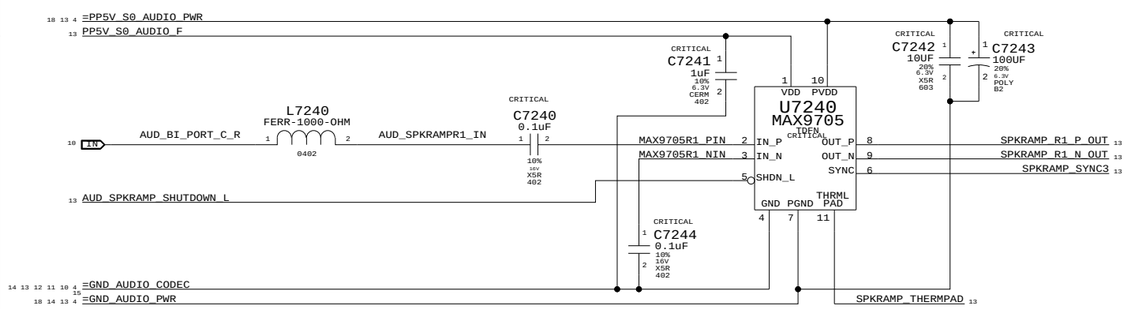
SPEAKER AMPLIFIERS (MAX9705) APN: 353S1355 TURN ON TIME: 30MS
Gain = 6dB 80 < FC < 132Hz TURN ON DELAY: 60MS



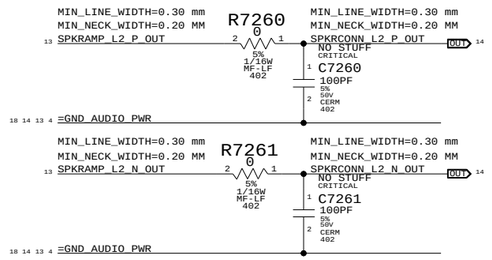


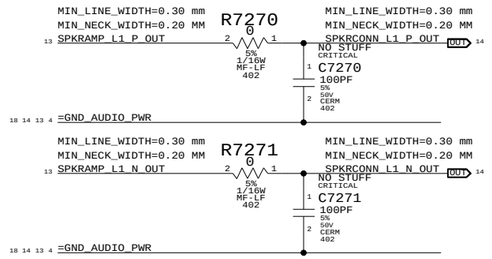
XW7200
SM
=GND_AUDIO_CODEC — SPKRAMP_THERMPAD



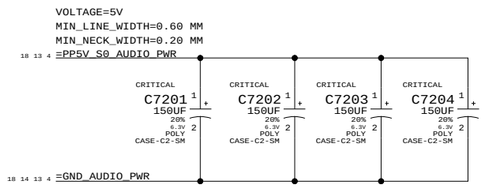


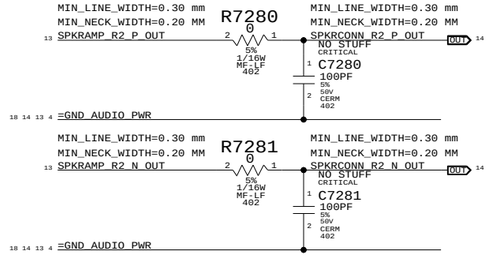
EMI FILTERS FOR AMPLIFIER OUTPUTS

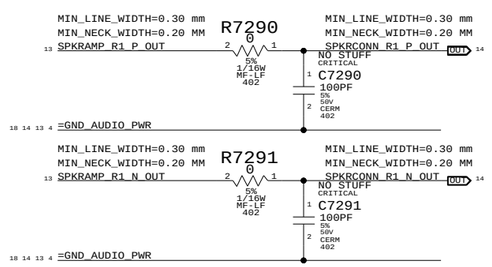




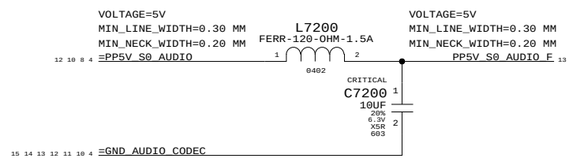
POWER AMPLIFIER SUPPLY BULK CAPS







ANALOG POWER RAIL



AUDIO: SPEAKER AMP

SYNC_MASTER=AUDIO_M9_PRO_LIO SYNC_DATE=01/06/2006

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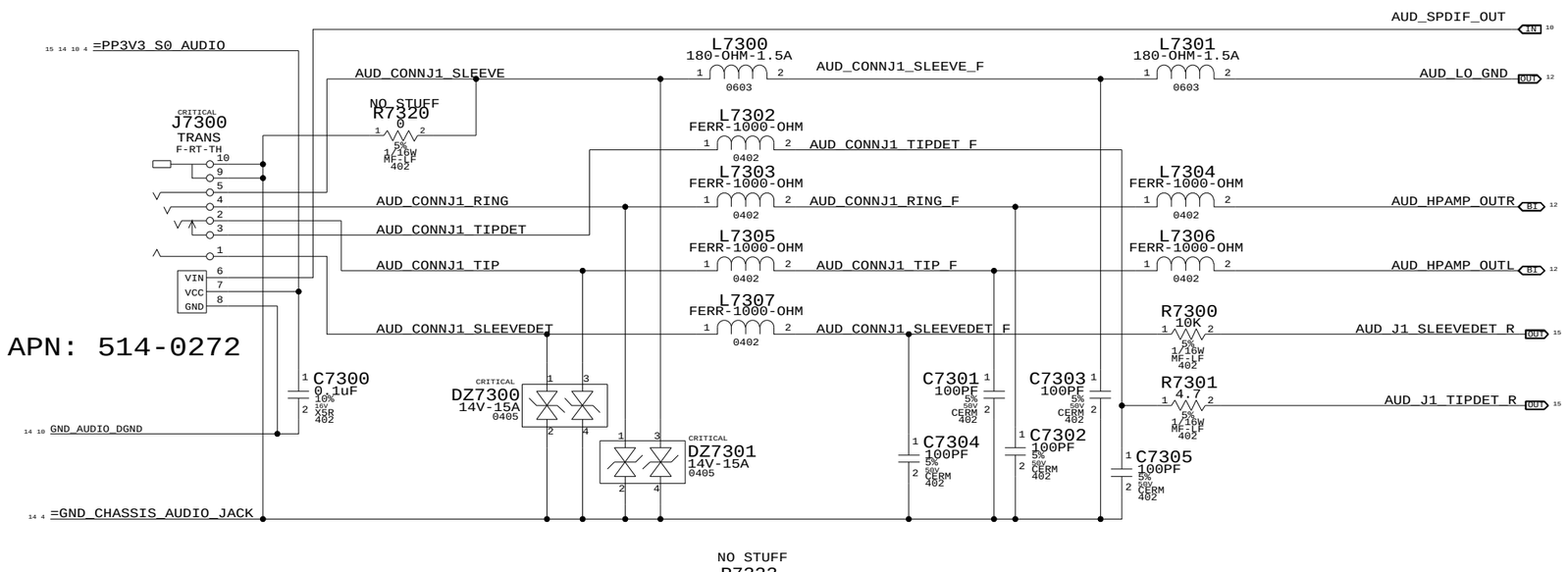
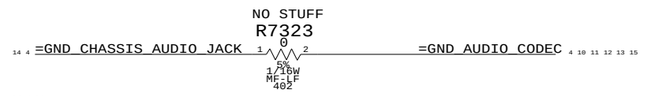
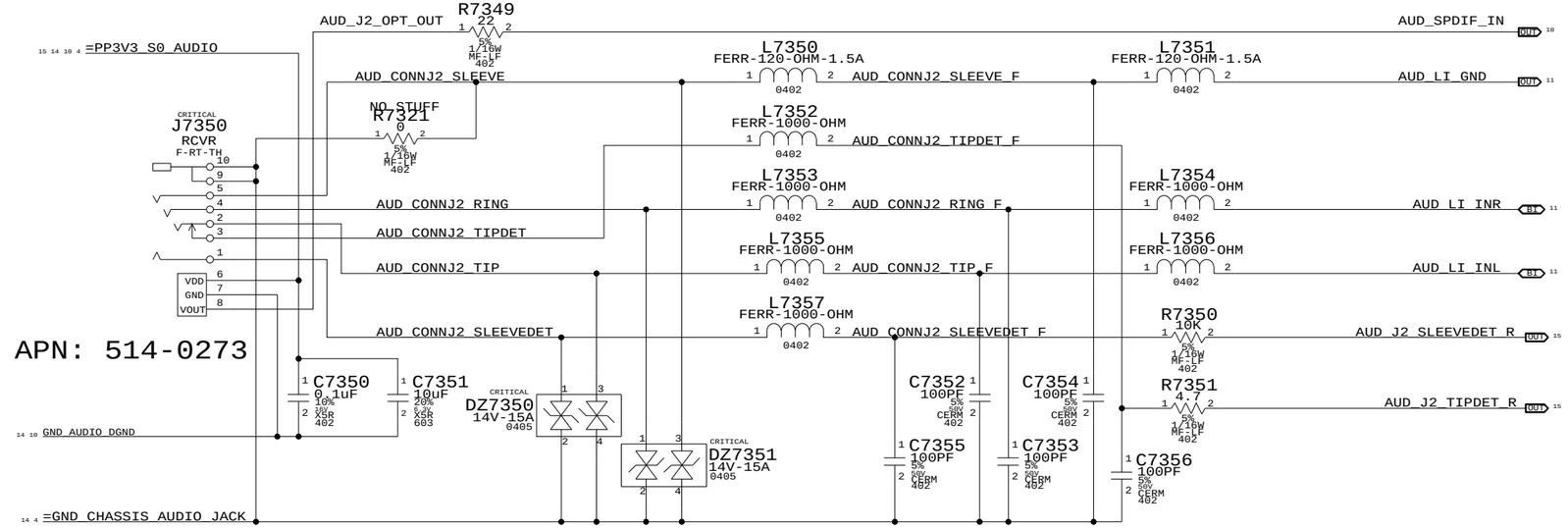
AUDIO JACK 1/DEFAULT LO/HP CONNECTOR, SPDIF TX

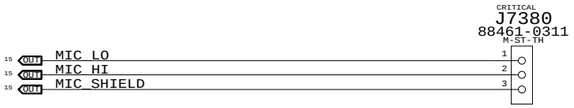




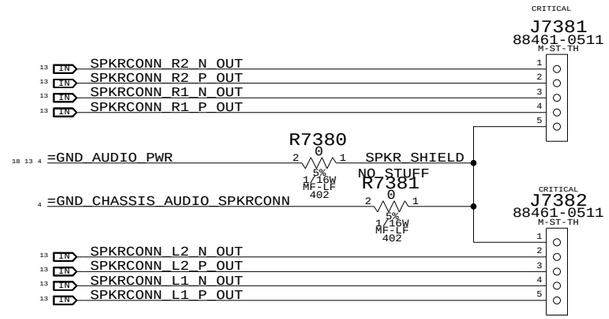


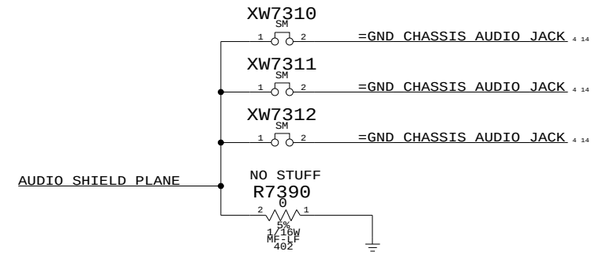
AUDIO JACK 2/DEFAULT LINE IN CONNECTOR, SPDIF RX

MIC CONNECTOR
APN: 518-0230



SPEAKER CONNECTORS
APN: 518-0229





AUDIO SHIELD
(FILLED SHAPE)

AUDIO: JACKS

SYNC_MASTER=AUDIO_M9_PRO_LIO SYNC_DATE=01/19/2006

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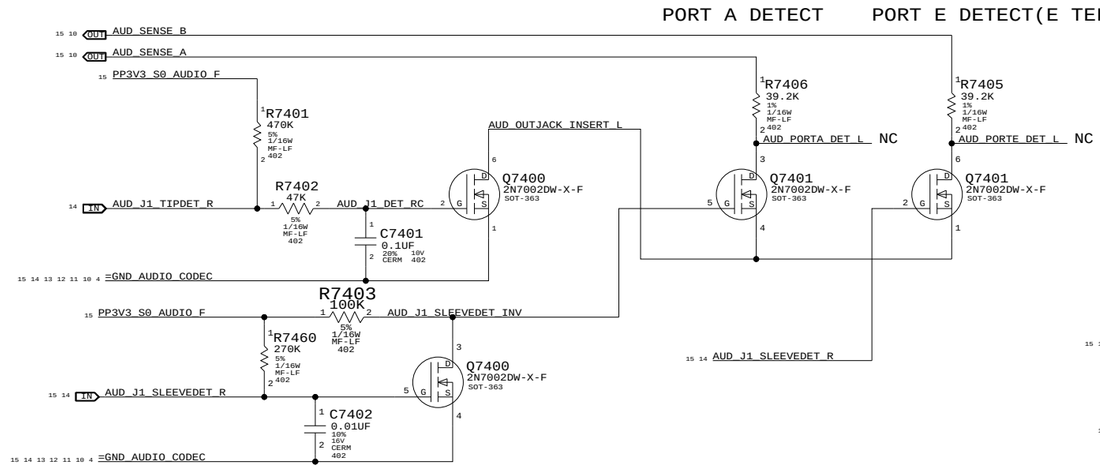
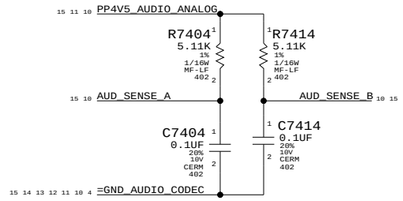
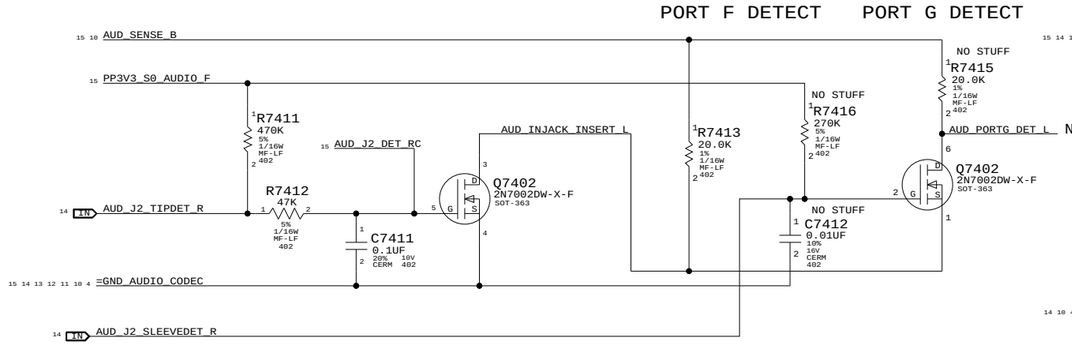
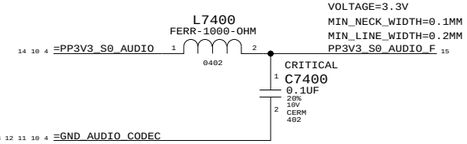






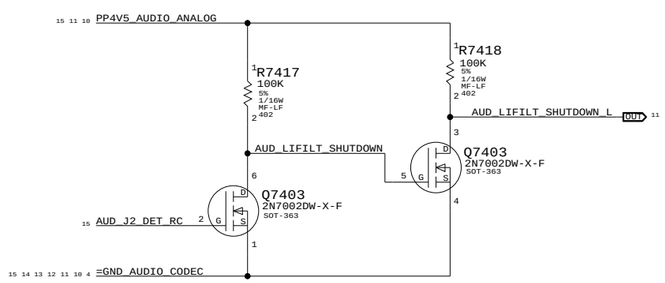


PLACE L7400/C7400 CLOSE TO Q7400

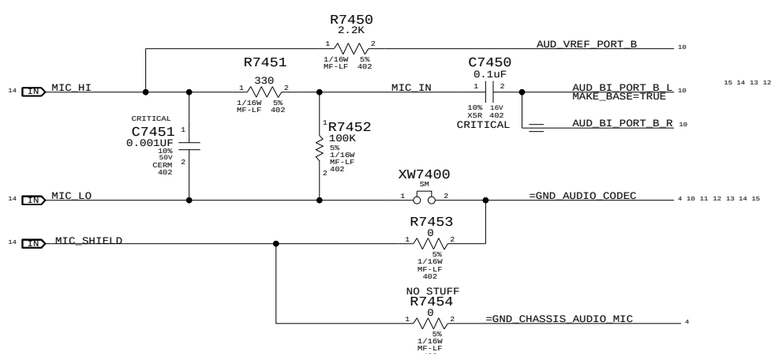
CODEC PORT ASSIGNMENTS

PORT A :HEADPHONE/LINE OUT
PORT B :MICROPHONE ON BOTH CH (ADC 0)
PORT C :TRANSDUCER 1 ON LEFT/RIGHT SPEAKER
PORT D :TRANSDUCER 2 ON LEFT/RIGHT SPEAKER
PORT E :SW USES TO TRIGGER DIGITAL OUT
PORT F :LINE IN (ADC 1)
CD INPUT :UNUSED

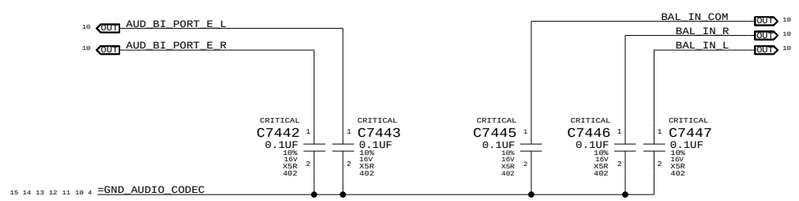
LINE IN FILTER SHUTDOWN CONTROL



MIC INPUT CIRCUITRY



UNUSED CODEC ANALOG PORT TERMINATIONS



AUDIO: JACK TRANSLATORS

SYNC_MASTER=AUDIO_M9_PRO_LIO
SYNC_DATE=01/06/2006

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3.3V S3/S0 Power Supply

=PPVIN_S3_3V3S3

=PP5V_S5_3V3S3

C7801 1uF 10% 25V X5R 603

R7830 2.2 5% 1/16W MF-LF 402

R7802 NO STUFF 0 5% 1/16W MF-LF 402

PP5V_S3_3V3S3_VCC
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.20mm

C7800 2.2uF 10% 6.3V CERM1 603

C7802 2.2uF 20% 6.3V CERM1 603

R7804 NO STUFF 0 5% 1/16W MF-LF 402

U7800 ISL6269 QFN

VIN
FSET
EN
FCCM
PGOOD
COMP
FB
VO
THRML PAD
UG
BOOT
PHASE
ISEN
LG
PVCC
VCC
PGND

3V3S3_UG
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.20mm

3V3S3_BOOT
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.20mm

R7823 0 5% 1/16W MF-LF 402

3V3S3_BOOT_R
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.20mm

C7809 0.22uF 20% 6.3V CERM 402

3V3S3_PHASE
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.20mm
SWITCH_NODE=TRUE

R7810 5.90K 1% 1/16W MF-LF 402

3V3S3_ISEN

3V3S3_LG
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.20mm

CRITICAL Q7800 FDM6296 MICROFET3X3

CRITICAL L7800 4.7UH IHLP

C7830 22uF 20% 16V X7R 1210

CRITICAL D7800 SMD MMBRM140XXG

NO STUFF C7822 0.001uF 10% 50V CERM 402

CRITICAL Q7801 FDM6296 MICROFET3X3

=LIO_P3V3S3_EN

NC_LIO_P3V3S3_PGOOD
NO_TEST=TRUE

3V3S3_FSET

3V3S3_FCCM

3V3S3_COMP

3V3S3_FB

3V3S3_COMP_R

R7806 57.6K 1% 1/16W MF-LF 402

C7806 0.01UF 10% 16V CERM 402

R7808 46.4K 1% 1/16W MF-LF 402

C7807 27pF 5% 50V CERM 402

C7808 0.0022uF 10% 50V CERM 402

R7805 0 5% 1/16W MF-LF 402

XW7800 SM

GND_3V3S3_SGND
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.20mm

3.3V S0 FET

Q7890 FDC638P SM-LF

=PP3V3_S0_FET

LIO_P3V3S0_EN_L

R7890 0 5% 1/16W MF-LF 402

LIO_P3V3S0_EN_R_L
MIN_LINE_WIDTH=0.20mm
MIN_NECK_WIDTH=0.20mm

C7890 0.0022uF 10% 50V CERM 402

4.5A max, limited by L7800

=PP3V3_S3_REG

R7821 3.32K 1% 1/16W MF-LF 402

R7822 732 1% 1/16W MF-LF 402

R7800 0 5% 1/16W MF-LF 402

3V3S3_FB_R

NO STUFF C7843 0.01uF 10% 16V CERM 402

C7840 22uF 20% 6.3V X5R 805

C7842 22uF 20% 6.3V X5R 805

C7841 150UF 20% 6.3V POLY SMC-LF

3.3V Supply	
SYNC_MASTER=SIREN	SYNC_DATE=01/06/2006

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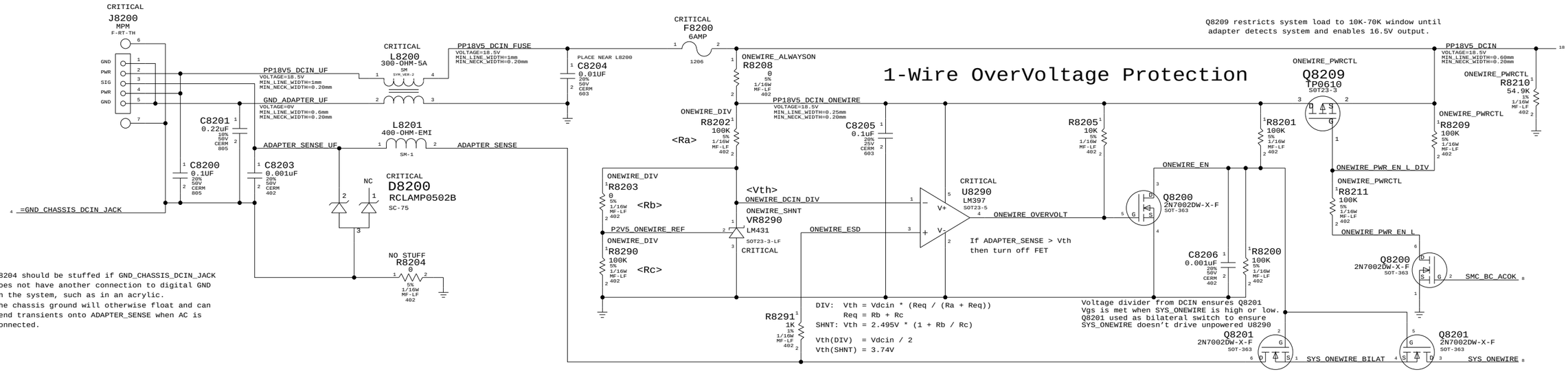
DC Power Jack



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0085	1	RES,6.2K,5%,1/16W,0402,LF	R8202		ONEWIRE_SHNT
114S0315	1	RES,10K,1%,1/16W,0402,LF	R8203		ONEWIRE_SHNT
114S0343	1	RES,20K,1%,1/16W,0402,LF	R8290		ONEWIRE_SHNT

ONEWIRE_SHNT BOM option allows the use of an adjustable shunt voltage regulator to provide the reference to the LM397 comparator. This allows the protection circuit to enforce a ~3.7V max signal on ADAPTER_SENSE instead of the voltage divider DCIN/2 approach.

R8202 value ensures 1mA current for DCIN >= 13.4V per LM431 spec.

DC-In & Battery Connectors

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE: NONE SHT 82 OF 87

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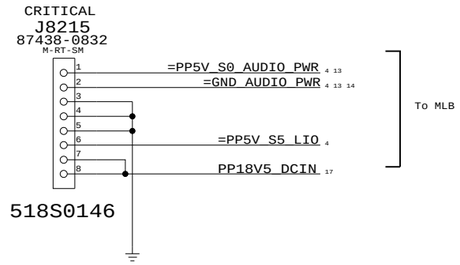
Left I/O Power Connector



LEFT I/O POWER CONNECTOR

SYNC_MASTER=SIREN SYNC_DATE=01/06/2006

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7066	02

SCALE	SHT
NONE	84 OF 87

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Title: Basenet Report
Design: alt_lio
Date: Jan 19 16:34:21 2006

Base nets and synonyms for alt_lio_lib.ALT_LIO(@alt_lio_lib.alt_lio(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
3V3S3_BOOT	3V3S3_BOOT - @alt_lio_lib.ALT_LIO	16C5
3V3S3_BOOT_R	3V3S3_BOOT_R - @alt_lio_lib.ALT_LIO	16C5
3V3S3_COMP	3V3S3_COMP - @alt_lio_lib.ALT_LIO	16B6
3V3S3_COMP_R	3V3S3_COMP_R - @alt_lio_lib.ALT_LIO	16B7
3V3S3_FB	3V3S3_FB - @alt_lio_lib.ALT_LIO	16B6
3V3S3_FB_R	3V3S3_FB_R - @alt_lio_lib.ALT_LIO	16B2
3V3S3_FCCM	3V3S3_FCCM - @alt_lio_lib.ALT_LIO	16B6
3V3S3_FSET	3V3S3_FSET - @alt_lio_lib.ALT_LIO	16C6
3V3S3_ISEN	3V3S3_ISEN - @alt_lio_lib.ALT_LIO	16B5
3V3S3_LG	3V3S3_LG - @alt_lio_lib.ALT_LIO	16B5
3V3S3_PHASE	3V3S3_PHASE - @alt_lio_lib.ALT_LIO	16B4
3V3S3_UG	3V3S3_UG - @alt_lio_lib.ALT_LIO	16C5
5V_REG_IN	5V_REG_IN - @alt_lio_lib.ALT_LIO	10A4
=EXCARD_CLKREQ_L	=EXCARD_CLKREQ_L - @alt_lio_lib.ALT_LIO	4C5 8C6
	EXCARD_CLKREQ_L - @alt_lio_lib.ALT_LIO	4C4 6B2
=EXCARD_OC_L	=EXCARD_OC_L - @alt_lio_lib.ALT_LIO	4C5 8C6
	EXCARD_OC_L - @alt_lio_lib.ALT_LIO	4C4 6B4
=GND_AUDIO	=GND_AUDIO - @alt_lio_lib.ALT_LIO	4A8 8B6
	=GND_AUDIO_CODEC -	4A7 10A6 10B6 10D2 11B7
	@alt_lio_lib.ALT_LIO	12B6 12C6 13A8 13B2 13B6 13B8 13C8 13C8 14B5 15A3 15A4 15A8 15B5 15B8 15C5 15C8 15D8
	GND_AUDIO - @alt_lio_lib.ALT_LIO	4A7
	=GND_AUDIO_CODEC -	4A7 10A6 10B6 10D2 11B7
	@alt_lio_lib.ALT_LIO	12B6 12C6 13A8 13B2 13B6 13B8 13C8 13C8 14B5 15A3 15A4 15A8 15B5 15B8 15C5 15C8 15D8
=GND_AUDIO_PWR	=GND_AUDIO_PWR -	4B8 13A4 13A4 13A8 13B4
	@alt_lio_lib.ALT_LIO	13B4 13B8 13C2 13C4 13C4 13C4 13C8 13C8 13D4 14C3 18C4
	GND_AUDIO_PWR -	4B7
	@alt_lio_lib.ALT_LIO	
=GND_CHASSIS_AUDIO_J ACK	=GND_CHASSIS_AUDIO_JACK -	4A7 14A8 14B1 14B1 14B1
	@alt_lio_lib.ALT_LIO	14B7 14C8
	=GND_CHASSIS_AUDIO_MIC -	4A7 15A4
	@alt_lio_lib.ALT_LIO	
	CHASSIS_GND2 - @alt_lio_lib.ALT_LIO	4A8
=GND_CHASSIS_AUDIO_S PKRCONN	=GND_CHASSIS_AUDIO_SPKRCONN -	4A7 14C3
	@alt_lio_lib.ALT_LIO	
	CHASSIS_GND3 - @alt_lio_lib.ALT_LIO	4A8
=GND_CHASSIS_DCIN_JA CK	=GND_CHASSIS_DCIN_JACK -	4A7 17C8
	@alt_lio_lib.ALT_LIO	
	=GND_CHASSIS_LTUSB -	4A7 5A2 5C2
	@alt_lio_lib.ALT_LIO	
	CHASSIS_GND1 - @alt_lio_lib.ALT_LIO	4A8
	=GND_CHASSIS_LTUSB -	4A7 5A2 5C2
	@alt_lio_lib.ALT_LIO	
=GND_CHASSIS_LIO_FLE X	=GND_CHASSIS_LIO_FLEX -	4A7 8B3
	@alt_lio_lib.ALT_LIO	
	=GND_CHASSIS_PCIE_EXCARD -	4A7 6B2
	@alt_lio_lib.ALT_LIO	
	CHASSIS_GND4 - @alt_lio_lib.ALT_LIO	4A8
	=GND_CHASSIS_PCIE_EXCARD -	4A7 6B2
	@alt_lio_lib.ALT_LIO	
=LIO_P3V3S3_EN	=LIO_P3V3S3_EN -	4C4 8C6 16B8
	@alt_lio_lib.ALT_LIO	
	=USB_LEFT_PWRON -	4C2 5C8
	@alt_lio_lib.ALT_LIO	
	LIO_P3V3S3_EN -	4C3
	@alt_lio_lib.ALT_LIO	
	=USB_LEFT_PWRON -	4C2 5C8
	@alt_lio_lib.ALT_LIO	
=LT2USB_OC_L	=LT2USB_OC_L - @alt_lio_lib.ALT_LIO	4A3 8C6
	USB_LEFT2_OC_L -	4A5 5B7
	@alt_lio_lib.ALT_LIO	
=LTUSB_OC_L	=LTUSB_OC_L - @alt_lio_lib.ALT_LIO	4A3 8C6
	USB_LEFT_OC_L -	4A5 5B7
	@alt_lio_lib.ALT_LIO	
=MINI_CLKREQ_L	=MINI_CLKREQ_L -	4B5 8C6
	@alt_lio_lib.ALT_LIO	
	MINI_CLKREQ_L -	4B4 7C6
	@alt_lio_lib.ALT_LIO	
=PCIE_CLK100M_EXCARD _N	=PCIE_CLK100M_EXCARD_N -	4D5 8B1
	@alt_lio_lib.ALT_LIO	
	PCIE_CLK100M_EXCARD_N -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=PCIE_CLK100M_EXCARD _P	=PCIE_CLK100M_EXCARD_P -	4D5 8B1
	@alt_lio_lib.ALT_LIO	
	PCIE_CLK100M_EXCARD_P -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=PCIE_CLK100M_MINI_N	=PCIE_CLK100M_MINI_N -	4B5 8C1
	@alt_lio_lib.ALT_LIO	
	PCIE_CLK100M_MINI_N -	4B2 7C6
	@alt_lio_lib.ALT_LIO	
=PCIE_CLK100M_MINI_P	=PCIE_CLK100M_MINI_P -	4B5 8C1
	@alt_lio_lib.ALT_LIO	
	PCIE_CLK100M_MINI_P -	4B2 7C6
	@alt_lio_lib.ALT_LIO	
=PCIE_EXCARD_D2R_N	=PCIE_EXCARD_D2R_N -	4D5 8B3
	@alt_lio_lib.ALT_LIO	
	PCIE_EXCARD_D2R_N -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=PCIE_EXCARD_D2R_P	=PCIE_EXCARD_D2R_P -	4D5 8B3
	@alt_lio_lib.ALT_LIO	
	PCIE_EXCARD_D2R_P -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=PCIE_EXCARD_R2D_N	=PCIE_EXCARD_R2D_N -	4D5 8B3
	@alt_lio_lib.ALT_LIO	
	PCIE_EXCARD_R2D_N -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=PCIE_EXCARD_R2D_P	=PCIE_EXCARD_R2D_P -	4D5 8B3
	@alt_lio_lib.ALT_LIO	
	PCIE_EXCARD_R2D_P -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=PCIE_MINI_D2R_N	=PCIE_MINI_D2R_N -	4B5 8C3
	@alt_lio_lib.ALT_LIO	
	PCIE_MINI_D2R_N -	4B2 7C6
	@alt_lio_lib.ALT_LIO	
=PCIE_MINI_D2R_P	=PCIE_MINI_D2R_P -	4B5 8C3
	@alt_lio_lib.ALT_LIO	
	PCIE_MINI_D2R_P -	4B2 7C6
	@alt_lio_lib.ALT_LIO	
=PCIE_MINI_R2D_N	=PCIE_MINI_R2D_N -	4B5 8C3
	@alt_lio_lib.ALT_LIO	
	PCIE_MINI_R2D_N -	4B2 7B6
	@alt_lio_lib.ALT_LIO	
=PCIE_MINI_R2D_P	=PCIE_MINI_R2D_P -	4C5 8C3
	@alt_lio_lib.ALT_LIO	
	PCIE_MINI_R2D_P -	4C2 7B6
	@alt_lio_lib.ALT_LIO	
=PP1V5_S0_EXCARD	=PP1V5_S0_EXCARD -	4C7 6C7 6C8
	@alt_lio_lib.ALT_LIO	
	=PP1V5_S0_LIO -	4C8 8B3
	@alt_lio_lib.ALT_LIO	
	=PP1V5_S0_MINI -	4C7 7C2
	@alt_lio_lib.ALT_LIO	
	PP1V5_S0_LIO - @alt_lio_lib.ALT_LIO	4C7
	=PP1V5_S0_MINI -	4C7 7C2
	@alt_lio_lib.ALT_LIO	
	=PP1V5_S0_LIO -	4C8 8B3
	@alt_lio_lib.ALT_LIO	
=PP3V3_S0_AUDIO	=PP3V3_S0_AUDIO -	4B7 10A6 10D7 14B8 14D8
	@alt_lio_lib.ALT_LIO	15B5
	=PP3V3_S0_EXCARD -	4B7 6B4 6C7
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S0_FET -	4B8 16C1
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S0_MINI -	4B7 7D2
	@alt_lio_lib.ALT_LIO	
	PP3V3_S0_LIO - @alt_lio_lib.ALT_LIO	4C7
	=PP3V3_S0_MINI -	4B7 7D2
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S0_FET -	4B8 16C1
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S0_EXCARD -	4B7 6B4 6C7
	@alt_lio_lib.ALT_LIO	
=PP3V3_S3_EXCARD	=PP3V3_S3_EXCARD -	4C7 6A5 6B8 6C7 6C8
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S3_LFTALS -	4C7 9D6
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S3_REG -	4C8 16B1
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S3_MINI -	4C7 7C2
	@alt_lio_lib.ALT_LIO	
	PP3V3_S3_LIO - @alt_lio_lib.ALT_LIO	4C7
	=PP3V3_S3_REG -	4C8 16B1
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S3_MINI -	4C7 7C2
	@alt_lio_lib.ALT_LIO	
	=PP3V3_S3_LFTALS -	4C7 9D6
	@alt_lio_lib.ALT_LIO	
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO -	4B8 8B3 10A6 12D7 13B2
	@alt_lio_lib.ALT_LIO	
	PP5V_S0_AUDIO_LIO -	4B7
	@alt_lio_lib.ALT_LIO	
=PP5V_S0_AUDIO_PWR	=PP5V_S0_AUDIO_PWR -	4B8 13A8 13B8 13C2 13C8
	@alt_lio_lib.ALT_LIO	13D8 18C4
	PP5V_S0_AUDIO_PWR_LIO -	4B7
	@alt_lio_lib.ALT_LIO	
=PP5V_S5_3V3S3	=PP5V_S5_3V3S3 -	4B7 16C8
	@alt_lio_lib.ALT_LIO	
	=PP5V_S5_LIO - @alt_lio_lib.ALT_LIO	4B8 18C4
	=PP5V_S5_LTUSB -	4B7 5B8 5D7
	@alt_lio_lib.ALT_LIO	
	PP5V_S5_LIO - @alt_lio_lib.ALT_LIO	4B7
	=PP5V_S5_LTUSB -	4B7 5B8 5D7
	@alt_lio_lib.ALT_LIO	
	=PP5V_S5_LIO - @alt_lio_lib.ALT_LIO	4B8 18C4
=PPBUS_G3H_LIO_CONN	=PPBUS_G3H_LIO_CONN -	4D8 8B3
	@alt_lio_lib.ALT_LIO	
	=PPVIN_S3_3V3S3 -	4D6 16D8
	@alt_lio_lib.ALT_LIO	
	PPBUS_G3H_LIO_CONN -	4D7
	@alt_lio_lib.ALT_LIO	
	=PPVIN_S3_3V3S3 -	4D6 16D8
	@alt_lio_lib.ALT_LIO	
=SMBUS_EXCARD_SCL	=SMBUS_EXCARD_SCL -	4A2 6C3
	@alt_lio_lib.ALT_LIO	
	=SMBUS_SB_SCL -	4A4 8B6
	@alt_lio_lib.ALT_LIO	
	SMBUS_SB_SCL - @alt_lio_lib.ALT_LIO	4A2
=SMBUS_EXCARD_SDA	=SMBUS_EXCARD_SDA -	4A4 6C3
	@alt_lio_lib.ALT_LIO	
	=SMBUS_SB_SDA -	4A5 8B6
	@alt_lio_lib.ALT_LIO	
	SMBUS_SB_SDA - @alt_lio_lib.ALT_LIO	4A4
=SMBUS_MINI_SCL	=SMBUS_MINI_SCL -	4A2 7B3
	@alt_lio_lib.ALT_LIO	
	SMBUS_MINI_SCL -	4A3
	@alt_lio_lib.ALT_LIO	
=SMBUS_MINI_SDA	=SMBUS_MINI_SDA -	4A3 7B3
	@alt_lio_lib.ALT_LIO	
	SMBUS_MINI_SDA -	4A4
	@alt_lio_lib.ALT_LIO	
=USB2_EXCARD_N	=USB2_EXCARD_N -	4D5 8C3
	@alt_lio_lib.ALT_LIO	
	USB2_EXCARD_N -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=USB2_EXCARD_P	=USB2_EXCARD_P -	4D5 8C3
	@alt_lio_lib.ALT_LIO	
	USB2_EXCARD_P -	4D2 6C3
	@alt_lio_lib.ALT_LIO	
=USB2_LT2_N	=USB2_LT2_N - @alt_lio_lib.ALT_LIO	4A3 8C3
	USB_LEFT2_N - @alt_lio_lib.ALT_LIO	4A5 5C5
=USB2_LT2_P	=USB2_LT2_P - @alt_lio_lib.ALT_LIO	4A3 8C3
	USB_LEFT2_P - @alt_lio_lib.ALT_LIO	4A5 5C5
=USB2_LT_N	=USB2_LT_N - @alt_lio_lib.ALT_LIO	4A3 8C3
	USB_LEFT_N - @alt_lio_lib.ALT_LIO	4A5 5B5
=USB2_LT_P	=USB2_LT_P - @alt_lio_lib.ALT_LIO	4B3 8C3
	USB_LEFT_P - @alt_lio_lib.ALT_LIO	4B5 5B5
ACZ_BITCLK	ACZ_BITCLK - @alt_lio_lib.ALT_LIO	8B6 10D7
ACZ_RST_L	ACZ_RST_L - @alt_lio_lib.ALT_LIO	8B6 10C7
ACZ_SDATAIN<0>	ACZ_SDATAIN<0> -	8B6 10C7
	@alt_lio_lib.ALT_LIO	
ACZ_SDATAOUT	ACZ_SDATAOUT - @alt_lio_lib.ALT_LIO	8C6 10D7
ACZ_SYNC	ACZ_SYNC - @alt_lio_lib.ALT_LIO	8B6 10D7
ADAPTER_SENSE	ADAPTER_SENSE -	17D6
	@alt_lio_lib.ALT_LIO	
ADAPTER_SENSE_UF	ADAPTER_SENSE_UF -	17D7
	@alt_lio_lib.ALT_LIO	
AUDIO_SHIELD_PLANE	AUDIO_SHIELD_PLANE -	14B3
	@alt_lio_lib.ALT_LIO	
AUD_4V5_SHDN_L	AUD_4V5_SHDN_L -	10A4
	@alt_lio_lib.ALT_LIO	
AUD_ANALOG_FILT_1	AUD_ANALOG_FILT_1 -	10C4
	@alt_lio_lib.ALT_LIO	
AUD_ANALOG_FILT_2	AUD_ANALOG_FILT_2 -	10C4
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_A_L	AUD_BI_PORT_A_L -	10C1 12B7
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_A_R	AUD_BI_PORT_A_R -	10C1 12A7
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_B_L	AUD_BI_PORT_B_L -	10C1 15A4
	@alt_lio_lib.ALT_LIO	
	AUD_BI_PORT_B_R -	10C1 15A4
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_C_L	AUD_BI_PORT_C_L -	10C7 13C8
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_C_R	AUD_BI_PORT_C_R -	10C7 13A8
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_D_L	AUD_BI_PORT_D_L -	10C7 13D8
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_D_R	AUD_BI_PORT_D_R -	10C7 13B8
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_E_L	AUD_BI_PORT_E_L -	10C1 15B3
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_E_R	AUD_BI_PORT_E_R -	10C1 15B3
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_F_L	AUD_BI_PORT_F_L -	10C1 11C2
	@alt_lio_lib.ALT_LIO	
AUD_BI_PORT_F_R	AUD_BI_PORT_F_R -	10C1 11B2
	@alt_lio_lib.ALT_LIO	
AUD_BYPASS	AUD_BYPASS - @alt_lio_lib.ALT_LIO	10C4
AUD_CODEC_INREF	AUD_CODEC_INREF -	11B3
	@alt_lio_lib.ALT_LIO	
AUD_CODEC_OUTL_C	AUD_CODEC_OUTL_C -	12B6
	@alt_lio_lib.ALT_LIO	
AUD_CODEC_OUTL_R	AUD_CODEC_OUTL_R -	12B5
	@alt_lio_lib.ALT_LIO	
AUD_CODEC_OUTR_C	AUD_CODEC_OUTR_C -	12A6
	@alt_lio_lib.ALT_LIO	
AUD_CODEC_OUTR_R	AUD_CODEC_OUTR_R -	12A5
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_RING	AUD_CONNJ1_RING -	14C7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_RING_F	AUD_CONNJ1_RING_F -	14C6
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_SLEEVE	AUD_CONNJ1_SLEEVE -	14D7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_SLEEVEDET	AUD_CONNJ1_SLEEVEDET -	14C7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_SLEEVEDET _F	AUD_CONNJ1_SLEEVEDET_F -	14C6
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_SLEEVE_F	AUD_CONNJ1_SLEEVE_F -	14D6
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_TIP	AUD_CONNJ1_TIP -	14C7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_TIPDET	AUD_CONNJ1_TIPDET -	14C7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_TIPDET_F	AUD_CONNJ1_TIPDET_F -	14D6
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ1_TIP_F	AUD_CONNJ1_TIP_F -	14C6
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_RING	AUD_CONNJ2_RING -	14B7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_RING_F	AUD_CONNJ2_RING_F -	14B5
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_SLEEVE	AUD_CONNJ2_SLEEVE -	14B7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_SLEEVEDET	AUD_CONNJ2_SLEEVEDET -	14A7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_SLEEVEDET _F	AUD_CONNJ2_SLEEVEDET_F -	14A5
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_SLEEVE_F	AUD_CONNJ2_SLEEVE_F -	14B5
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_TIP	AUD_CONNJ2_TIP -	14B7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_TIPDET	AUD_CONNJ2_TIPDET -	14B7
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_TIPDET_F	AUD_CONNJ2_TIPDET_F -	14B5
	@alt_lio_lib.ALT_LIO	
AUD_CONNJ2_TIP_F	AUD_CONNJ2_TIP_F -	14B5
	@alt_lio_lib.ALT_LIO	
AUD_GPIO_0	AUD_GPIO_0 - @alt_lio_lib.ALT_LIO	10B8 13D8
AUD_GPIO_0_R	AUD_GPIO_0_R - @alt_lio_lib.ALT_LIO	10B7 10C7
AUD_GPIO_1	AUD_GPIO_1 - @alt_lio_lib.ALT_LIO	10B8 12C7
AUD_GPIO_1_R	AUD_GPIO_1_R - @alt_lio_lib.ALT_LIO	10B7 10C7
AUD_HPAMP_INL_M	AUD_HPAMP_INL_M -	12B3 12D7
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_INL_P	AUD_HPAMP_INL_P -	12B3 12D7
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_INR_M	AUD_HPAMP_INR_M -	12A3 12C7
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_INR_P	AUD_HPAMP_INR_P -	12A3 12C7
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_MUTE_L	AUD_HPAMP_MUTE_L -	12C6
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_OUTL	AUD_HPAMP_OUTL -	12D2 14C3
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_OUTL_R	AUD_HPAMP_OUTL_R -	12B3 12D2
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_OUTR	AUD_HPAMP_OUTR -	12C2 14C3
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_OUTR_R	AUD_HPAMP_OUTR_R -	12A3 12C2
	@alt_lio_lib.ALT_LIO	
AUD_HPAMP_REF	AUD_HPAMP_REF -	12B3 12C5 12D2
	@alt_lio_lib.ALT_LIO	
AUD_INJACK_INSERT_L	AUD_INJACK_INSERT_L -	15C7
	@alt_lio_lib.ALT_LIO	
AUD_J1_DET_RC	AUD_J1_DET_RC -	15D7
	@alt_lio_lib.ALT_LIO	
AUD_J1_SLEEVEDET_INV	AUD_J1_SLEEVEDET_INV -	15C7
	@alt_lio_lib.ALT_LIO	
AUD_J1_SLEEVEDET_R	AUD_J1_SLEEVEDET_R -	14C3 15C6 15C8
	@alt_lio_lib.ALT_LIO	
AUD_J1_TIPDET_R	AUD_J1_TIPDET_R -	14C3 15D8
	@alt_lio_lib.ALT_LIO	
AUD_J2_DET_RC	AUD_J2_DET_RC -	15A8 15C7
	@alt_lio_lib.ALT_LIO	
AUD_J2_OPT_OUT	AUD_J2_OPT_OUT -	14B7
	@alt_lio_lib.ALT_LIO	
AUD_J2_SLEEVEDET_R	AUD_J2_SLEEVEDET_R -	14A3 15B8
	@alt_lio_lib.ALT_LIO	
AUD_J2_TIPDET_R	AUD_J2_TIPDET_R -	14A3 15B8
	@alt_lio_lib.ALT_LIO	
AUD_LIFILT_LT	AUD_LIFILT_LT -	11C4
	@alt_lio_lib.ALT_LIO	
AUD_LIFILT_LT_R	AUD_LIFILT_LT_R -	11C5
	@alt_lio_lib.ALT_LIO	
AUD_LIFILT_RT	AUD_LIFILT_RT -	11B4
	@alt_lio_lib.ALT_LIO	
AUD_LIFILT_RT_R	AUD_LIFILT_RT_R -	11B5
	@alt_lio_lib.ALT_LIO	
AUD_LIFILT_SHUTDOWN	AUD_LIFILT_SHUTDOWN -	15A8
	@alt_lio_lib.ALT_LIO	
AUD_LIFILT_SHUTDOWN_ L	AUD_LIFILT_SHUTDOWN_L -	11C2 15A6
	@alt_lio_lib.ALT_LIO	
AUD_LI_GND	AUD_LI_GND - @alt_lio_lib.ALT_LIO	11C7 14B3
AUD_LI_INL	AUD_LI_INL - @alt_lio_lib.ALT_LIO	11C7 14B3
AUD_LI_INL_C	AUD_LI_INL_C - @alt_lio_lib.ALT_LIO	11C5
AUD_LI_INL_C_R	AUD_LI_INL_C_R -	11C4
	@alt_lio_lib.ALT_LIO	
AUD_LI_INR	AUD_LI_INR - @alt_lio_lib.ALT_LIO	11B7 14B3
AUD_LI_INR_C	AUD_LI_INR_C - @alt_lio_lib.ALT_LIO	11B5
AUD_LI_INR_C_R	AUD_LI_INR_C_R -	11B4
	@alt_lio_lib.ALT_LIO	
AUD_LO_GND	AUD_LO_GND - @alt_lio_lib.ALT_LIO	12C2 14D3
AUD_OUTJACK_INSERT_L	AUD_OUTJACK_INSERT_L -	15D7
	@alt_lio_lib.ALT_LIO	
AUD_PORTA_DET_L	AUD_PORTA_DET_L -	15D5
	@alt_lio_lib.ALT_LIO	
AUD_PORTE_DET_L	AUD_PORTE_DET_L -	15D5
	@alt_lio_lib.ALT_LIO	
AUD_PORTF_L	AUD_PORTF_L - @alt_lio_lib.ALT_LIO	11C3
AUD_PORTF_R	AUD_PORTF_R - @alt_lio_lib.ALT_LIO	11B3
AUD_PORTG_DET_L	AUD_PORTG_DET_L -	15C5
	@alt_lio_lib.ALT_LIO	
AUD_SENSE_A	AUD_SENSE_A - @alt_lio_lib.ALT_LIO	10C1 15C5 15D8
AUD_SENSE_B	AUD_SENSE_B - @alt_lio_lib.ALT_LIO	10C1 15C4 15C8 15D8
AUD_SPDIF_IN	AUD_SPDIF_IN - @alt_lio_lib.ALT_LIO	10C1 14B3
AUD_SPDIF_OUT	AUD_SPDIF_OUT -	10D1 14D3
	@alt_lio_lib.ALT_LIO	
AUD_SPDIF_OUT_R	AUD_SPDIF_OUT_R -	10D4
	@alt_lio_lib.ALT_LIO	
AUD_SPKRAMPL1_IN	AUD_SPKRAMPL1_IN -	13C7
	@alt_lio_lib.ALT_LIO	
AUD_SPKRAMPL2_IN	AUD_SPKRAMPL2_IN -	13D7
	@alt_lio_lib.ALT_LIO	
AUD_SPKRAMPR1_IN	AUD_SPKRAMPR1_IN -	13A7
	@alt_lio_lib.ALT_LIO	
AUD_SPKRAMPR2_IN	AUD_SPKRAMPR2_IN -	13B7
	@alt_lio_lib.ALT_LIO	
AUD_SPKRAMP_SHUTDOWN _L	AUD_SPKRAMP_SHUTDOWN_L -	13A8 13B8 13C8 13D8
	@alt_lio_lib.ALT_LIO	
AUD_VREF_FILT	AUD_VREF_FILT -	10C4
	@alt_lio_lib.ALT_LIO	
AUD_VREF_PORT_B	AUD_VREF_PORT_B -	10C1 15A4
	@alt_lio_lib.ALT_LIO	
AUD_VREF_PORT_C	AUD_VREF_PORT_C -	10C1 11B2
	@alt_lio_lib.ALT_LIO	
BAL_IN_COM	BAL_IN_COM - @alt_lio_lib.ALT_LIO	10C7 15B1
BAL_IN_L	BAL_IN_L - @alt_lio_lib.ALT_LIO	10C7 15B1
BAL_IN_R	BAL_IN_R - @alt_lio_lib.ALT_LIO	10C7 15B1
BEEP	BEEP - @alt_lio_lib.ALT_LIO	10C6
EXCARD_CLKREQ_CONN	EXCARD_CLKREQ_CONN -	6B3
	@alt_lio_lib.ALT_LIO	
EXCARD_CLKREQ_CONN_L	EXCARD_CLKREQ_CONN_L -	6A4 6C3
	@alt_lio_lib.ALT_LIO	
EXCARD_CPPE_L	EXCARD_CPPE_L -	6A8 6C3 6C3
	@alt_lio_lib.ALT_LIO	
EXCARD_CPUSB_L	EXCARD_CPUSB_L -	6A8 6C3 6C3
	@alt_lio_lib.ALT_LIO	
EXCARD_OC_OUT_L	EXCARD_OC_OUT_L -	6A6
	@alt_lio_lib.ALT_LIO	
EXCARD_PRESENT	EXCARD_PRESENT -	6A6
	@alt_lio_lib.ALT_LIO	
EXCARD_RCLKEN	EXCARD_RCLKEN -	6B3 6C5
	@alt_lio_lib.ALT_LIO	
EXCARD_SHDN_L_R	EXCARD_SHDN_L_R -	6C6
	@alt_lio_lib.ALT_LIO	
GND_3V3S3_SGND	GND_3V3S3_SGND -	16B7
	@alt_lio_lib.ALT_LIO	
GND_ADAPTER_UF	GND_ADAPTER_UF -	17D7
	@alt_lio_lib.ALT_LIO	
GND_AUDIO_DGND	GND_AUDIO_DGND -	10A6 10A7 10B7 10D7 14A8
	@alt_lio_lib.ALT_LIO	14C8
GND_AUDIO_HPAMP_PGND	GND_AUDIO_HPAMP_PGND -	12C5
	@alt_lio_lib.ALT_LIO	
LEFT_ALS_GAIN_SW	LEFT_ALS_GAIN_SW -	8C6 9C4
	@alt_lio_lib.ALT_LIO	
LEFT_ALS_GAIN_SW_R	LEFT_ALS_GAIN_SW_R -	9C5
	@alt_lio_lib.ALT_LIO	
LEFT_ALS_OP_COMP	LEFT_ALS_OP_COMP -	9C6
	@alt_lio_lib.ALT_LIO	
LEFT_ALS_OP_IN	LEFT_ALS_OP_IN -	9C5
	@alt_lio_lib.ALT_LIO	
LEFT_ALS_OUT	LEFT_ALS_OUT - @alt_lio_lib.ALT_LIO	8C6 9C4
LEFT_ALS_OUT_FB	LEFT_ALS_OUT_FB -	9C5
	@alt_lio_lib.ALT_LIO	
LEFT_GAIN_SETTING	LEFT_GAIN_SETTING -	9C5
	@alt_lio_lib.ALT_LIO	
LEFT_PHOTODIODE	LEFT_PHOTODIODE -	9C6
	@alt_lio_lib.ALT_LIO	
LIO_P3V3S0_EN_L	LIO_P3V3S0_EN_L -	8C6 16C3
	@alt_lio_lib.ALT_LIO	
LIO_P3V3S0_EN_R_L	LIO_P3V3S0_EN_R_L -	16C2
	@alt_lio_lib.ALT_LIO	
LIO_PLT_RESET_L	LIO_PLT_RESET_L -	4C3 8C6
	@alt_lio_lib.ALT_LIO	
	PLT_RESET_L - @alt_lio_lib.ALT_LIO	4C4 6C7 7C3
MAX9705L1_NIN	MAX9705L1_NIN -	13C6
	@alt_lio_lib.ALT_LIO	
MAX9705L1_PIN	MAX9705L1_PIN -	13C6
	@alt_lio_lib.ALT_LIO	
MAX9705L2_NIN	MAX9705L2_NIN -	13D6
	@alt_lio_lib.ALT_LIO	
MAX9705L2_PIN	MAX9705L2_PIN -	13D6
	@alt_lio_lib.ALT_LIO	
MAX9705R1_NIN	MAX9705R1_NIN -	13A6
	@alt_lio_lib.ALT_LIO	
MAX9705R1_PIN	MAX9705R1_PIN -	13A6
	@alt_lio_lib.ALT_LIO	
MAX9705R2_NIN	MAX9705R2_NIN -	13B6
	@alt_lio_lib.ALT_LIO	
MAX9705R2_PIN	MAX9705R2_PIN

MIC_SHIELD	MIC_SHIELD - @alt_lio_lib.ALT_LIO	14D3 15A6
NC_AUD_GPIO_2	NC_AUD_GPIO_2 - @alt_lio_lib.ALT_LIO	10C7
NC_LED_WLAN_L	NC_LED_WLAN_L - @alt_lio_lib.ALT_LIO	7B3
NC_LED_WPAN_L	NC_LED_WPAN_L - @alt_lio_lib.ALT_LIO	7B3
NC_LED_WWAN_L	NC_LED_WWAN_L - @alt_lio_lib.ALT_LIO	7B3
NC_LIO_P3V3S3_PGOOD	NC_LIO_P3V3S3_PGOOD - @alt_lio_lib.ALT_LIO	16B8
NC_UIM_CLK	NC_UIM_CLK - @alt_lio_lib.ALT_LIO	7C3
NC_UIM_DATA	NC_UIM_DATA - @alt_lio_lib.ALT_LIO	7C3
NC_UIM_PWR	NC_UIM_PWR - @alt_lio_lib.ALT_LIO	7C3
NC_UIM_RESET	NC_UIM_RESET - @alt_lio_lib.ALT_LIO	7C3
NC_UIM_VPP	NC_UIM_VPP - @alt_lio_lib.ALT_LIO	7C3
NC_VOL_DOWN	NC_VOL_DOWN - @alt_lio_lib.ALT_LIO	10C7
NC_VOL_UP	NC_VOL_UP - @alt_lio_lib.ALT_LIO	10C7
NC_W_DISABLE_L	NC_W_DISABLE_L - @alt_lio_lib.ALT_LIO	7C3
ONEWIRE_DCIN_DIV	ONEWIRE_DCIN_DIV - @alt_lio_lib.ALT_LIO	17C5
ONEWIRE_EN	ONEWIRE_EN - @alt_lio_lib.ALT_LIO	17D3
ONEWIRE_ESD	ONEWIRE_ESD - @alt_lio_lib.ALT_LIO	17C4
ONEWIRE_OVERVOLT	ONEWIRE_OVERVOLT - @alt_lio_lib.ALT_LIO	17C4
ONEWIRE_PWR_EN_L	ONEWIRE_PWR_EN_L - @alt_lio_lib.ALT_LIO	17C2
ONEWIRE_PWR_EN_L_DIV	ONEWIRE_PWR_EN_L_DIV - @alt_lio_lib.ALT_LIO	17D2
P2V5_ONEWIRE_REF	P2V5_ONEWIRE_REF - @alt_lio_lib.ALT_LIO	17C5
PCIE_CLK100M_EXCARD_UF_N	PCIE_CLK100M_EXCARD_UF_N - @alt_lio_lib.ALT_LIO	8C4
PCIE_CLK100M_EXCARD_UF_P	PCIE_CLK100M_EXCARD_UF_P - @alt_lio_lib.ALT_LIO	8B4
PCIE_CLK100M_MINI_UF_N	PCIE_CLK100M_MINI_UF_N - @alt_lio_lib.ALT_LIO	8C4
PCIE_CLK100M_MINI_UF_P	PCIE_CLK100M_MINI_UF_P - @alt_lio_lib.ALT_LIO	8C4
PCIE_WAKE_EXCARD_L	PCIE_WAKE_EXCARD_L - @alt_lio_lib.ALT_LIO	4C3 6C3
	PCIE_WAKE_L - @alt_lio_lib.ALT_LIO	4C4 8C6
	PCIE_WAKE_MINI_L - @alt_lio_lib.ALT_LIO	4C3 7C6
	PCIE_WAKE_L - @alt_lio_lib.ALT_LIO	4C4 8C6
PLT_RESET_SWITCH_L	PLT_RESET_SWITCH_L - @alt_lio_lib.ALT_LIO	6C3 6C3
PP1V5_S0_EXCARD_SWITCH	PP1V5_S0_EXCARD_SWITCH - @alt_lio_lib.ALT_LIO	6C3 6C3
PP3V3_AUDIO_CODEC	PP3V3_AUDIO_CODEC - @alt_lio_lib.ALT_LIO	10D6
PP3V3_S0_AUDIO_F	PP3V3_S0_AUDIO_F - @alt_lio_lib.ALT_LIO	15B4 15C8 15C8 15D8
PP3V3_S0_EXCARD_SWITCH	PP3V3_S0_EXCARD_SWITCH - @alt_lio_lib.ALT_LIO	6C3 6C3
PP3V3_S3_EXCARD_SWITCH	PP3V3_S3_EXCARD_SWITCH - @alt_lio_lib.ALT_LIO	6C3 6C3
PP4V5_AUDIO_ANALOG	PP4V5_AUDIO_ANALOG - @alt_lio_lib.ALT_LIO	10A2 10D2 11C7 15A8 15C5
PP4V5_AUDIO_ANALOG_F	PP4V5_AUDIO_ANALOG_F - @alt_lio_lib.ALT_LIO	10D5
PP4V5_AUDIO_ANALOG_F1	PP4V5_AUDIO_ANALOG_F1 - @alt_lio_lib.ALT_LIO	10D5
PP5V_AUDIO_HPAMP_AVDD_F	PP5V_AUDIO_HPAMP_AVDD_F - @alt_lio_lib.ALT_LIO	12D4
PP5V_AUDIO_HPAMP_PVDD_F	PP5V_AUDIO_HPAMP_PVDD_F - @alt_lio_lib.ALT_LIO	12D5
PP5V_PWRON_USB_LEFT2_EMI	PP5V_PWRON_USB_LEFT2_EMI - @alt_lio_lib.ALT_LIO	5D4
PP5V_PWRON_USB_LEFT_EMI	PP5V_PWRON_USB_LEFT_EMI - @alt_lio_lib.ALT_LIO	5B4
PP5V_S0_AUDIO_F	PP5V_S0_AUDIO_F - @alt_lio_lib.ALT_LIO	13A8 13B1 13B8 13C8 13D8
PP5V_S3_3V3S3_R	PP5V_S3_3V3S3_R - @alt_lio_lib.ALT_LIO	16C6
PP5V_S3_3V3S3_VCC	PP5V_S3_3V3S3_VCC - @alt_lio_lib.ALT_LIO	16C7
PP5V_S3_USB_SWITCH_OUT1	PP5V_S3_USB_SWITCH_OUT1 - @alt_lio_lib.ALT_LIO	5B5
PP5V_S3_USB_SWITCH_OUT2	PP5V_S3_USB_SWITCH_OUT2 - @alt_lio_lib.ALT_LIO	5D5
PP18V5_DCIN	PP18V5_DCIN - @alt_lio_lib.ALT_LIO	17D1 18C4
PP18V5_DCIN_FUSE	PP18V5_DCIN_FUSE - @alt_lio_lib.ALT_LIO	17D6
PP18V5_DCIN_ONEWIRE	PP18V5_DCIN_ONEWIRE - @alt_lio_lib.ALT_LIO	17D5
PP18V5_DCIN_UF	PP18V5_DCIN_UF - @alt_lio_lib.ALT_LIO	17D7
SDATAIN	SDATAIN - @alt_lio_lib.ALT_LIO	10C6
SMC_BC_ACOK	SMC_BC_ACOK - @alt_lio_lib.ALT_LIO	8C6 17C1
SMC_EXCARD_CP	SMC_EXCARD_CP - @alt_lio_lib.ALT_LIO	6A4 8C6
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @alt_lio_lib.ALT_LIO	6C7 8C6
SPKRAMP_L1_N_OUT	SPKRAMP_L1_N_OUT - @alt_lio_lib.ALT_LIO	13C4 13C5
SPKRAMP_L1_P_OUT	SPKRAMP_L1_P_OUT - @alt_lio_lib.ALT_LIO	13C4 13C5
SPKRAMP_L2_N_OUT	SPKRAMP_L2_N_OUT - @alt_lio_lib.ALT_LIO	13D4 13D5
SPKRAMP_L2_P_OUT	SPKRAMP_L2_P_OUT - @alt_lio_lib.ALT_LIO	13D4 13D5
SPKRAMP_R1_N_OUT	SPKRAMP_R1_N_OUT - @alt_lio_lib.ALT_LIO	13A4 13A5
SPKRAMP_R1_P_OUT	SPKRAMP_R1_P_OUT - @alt_lio_lib.ALT_LIO	13A4 13A5
SPKRAMP_R2_N_OUT	SPKRAMP_R2_N_OUT - @alt_lio_lib.ALT_LIO	13B4 13B5
SPKRAMP_R2_P_OUT	SPKRAMP_R2_P_OUT - @alt_lio_lib.ALT_LIO	13B4 13B5
SPKRAMP_SYNC1	SPKRAMP_SYNC1 - @alt_lio_lib.ALT_LIO	13C5 13D5
SPKRAMP_SYNC2	SPKRAMP_SYNC2 - @alt_lio_lib.ALT_LIO	13B5 13C5
SPKRAMP_SYNC3	SPKRAMP_SYNC3 - @alt_lio_lib.ALT_LIO	13A5 13B5
SPKRAMP_THERMPAD	SPKRAMP_THERMPAD - @alt_lio_lib.ALT_LIO	13A5 13B5 13B5 13C5 13C5
SPKRCONN_L1_N_OUT	SPKRCONN_L1_N_OUT - @alt_lio_lib.ALT_LIO	13C3 14C3
SPKRCONN_L1_P_OUT	SPKRCONN_L1_P_OUT - @alt_lio_lib.ALT_LIO	13C3 14C3
SPKRCONN_L2_N_OUT	SPKRCONN_L2_N_OUT - @alt_lio_lib.ALT_LIO	13D3 14C3
SPKRCONN_L2_P_OUT	SPKRCONN_L2_P_OUT - @alt_lio_lib.ALT_LIO	13D3 14C3
SPKRCONN_R1_N_OUT	SPKRCONN_R1_N_OUT - @alt_lio_lib.ALT_LIO	13A3 14C3
SPKRCONN_R1_P_OUT	SPKRCONN_R1_P_OUT - @alt_lio_lib.ALT_LIO	13A3 14C3
SPKRCONN_R2_N_OUT	SPKRCONN_R2_N_OUT - @alt_lio_lib.ALT_LIO	13B3 14C3
SPKRCONN_R2_P_OUT	SPKRCONN_R2_P_OUT - @alt_lio_lib.ALT_LIO	13B3 14C3
SPKR_SHIELD	SPKR_SHIELD - @alt_lio_lib.ALT_LIO	14C2
SYS_ONEWIRE	SYS_ONEWIRE - @alt_lio_lib.ALT_LIO	8C6 17C1
SYS_ONEWIRE_BILAT	SYS_ONEWIRE_BILAT - @alt_lio_lib.ALT_LIO	17C2
TP_EXCARD_STBY_L	TP_EXCARD_STBY_L - @alt_lio_lib.ALT_LIO	6C7
TP_USB2_MINI_N	TP_USB2_MINI_N - @alt_lio_lib.ALT_LIO	4B2
	USB2_MINI_N - @alt_lio_lib.ALT_LIO	4B5 7B3
TP_USB2_MINI_P	TP_USB2_MINI_P - @alt_lio_lib.ALT_LIO	4B2
	USB2_MINI_P - @alt_lio_lib.ALT_LIO	4B5 7B3
USB_LEFT2_EMI_N	USB_LEFT2_EMI_N - @alt_lio_lib.ALT_LIO	5C4
USB_LEFT2_EMI_P	USB_LEFT2_EMI_P - @alt_lio_lib.ALT_LIO	5C4
USB_LEFT2_GND	USB_LEFT2_GND - @alt_lio_lib.ALT_LIO	5C3
USB_LEFT_EMI_N	USB_LEFT_EMI_N - @alt_lio_lib.ALT_LIO	5B4
USB_LEFT_EMI_P	USB_LEFT_EMI_P - @alt_lio_lib.ALT_LIO	5B4
USB_LEFT_GND	USB_LEFT_GND - @alt_lio_lib.ALT_LIO	5B3
USB_LEFT_PWRON_L	USB_LEFT_PWRON_L - @alt_lio_lib.ALT_LIO	5D7
VREG_FB	VREG_FB - @alt_lio_lib.ALT_LIO	10A3

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C5100	CAP_603	alt_lio[5B7]
C5101	CAP_402	alt_lio[5B7]
C5102	CAP_603	alt_lio[5B6]
C5103	CAP_P_CASE-C2-SM	alt_lio[5B5]
C5112	CAP_603	alt_lio[5C6]
C5113	CAP_P_CASE-C2-SM	alt_lio[5C5]
C5150	CAP_603	alt_lio[5B3]
C5151	CAP_603	alt_lio[5A3]
C5160	CAP_603	alt_lio[5D3]
C5161	CAP_603	alt_lio[5C3]
C5300	CAP_402	alt_lio[6C4]
C5301	CAP_402	alt_lio[6C4]
C5302	CAP_402	alt_lio[6C4]
C5303	CAP_603	alt_lio[6C4]
C5304	CAP_603	alt_lio[6C4]
C5305	CAP_603	alt_lio[6C4]
C5330	CAP_402	alt_lio[6C8]
C5331	CAP_603	alt_lio[6C7]
C5334	CAP_402	alt_lio[6C8]
C5335	CAP_603	alt_lio[6C7]
C5350	CAP_402	alt_lio[6A7]
C5351	CAP_402	alt_lio[6A5]
C5360	CAP_402	alt_lio[6A3]
C5400	CAP_402	alt_lio[7C3]
C5401	CAP_603	alt_lio[7C3]
C5410	CAP_402	alt_lio[7C3]
C5411	CAP_603	alt_lio[7C3]
C5420	CAP_402	alt_lio[7C3]
C5421	CAP_603	alt_lio[7C3]
C6401	CAP_402	alt_lio[9C6]
C6402	CAP_402	alt_lio[9C5]
C6403	CAP_402	alt_lio[9D5]
C6404	CAP_402	alt_lio[9B5]
C6800	CAP_603	alt_lio[10D6]
C6801	CAP_402	alt_lio[10D6]
C6802	CAP_603	alt_lio[10D4]
C6803	CAP_P_B2	alt_lio[10A3]
C6804	CAP_P_SMA-LF	alt_lio[10B4]
C6805	CAP_603	alt_lio[10B4]
C6806	CAP_603	alt_lio[10B3]
C6807	CAP_P_SMA-LF	alt_lio[10B3]
C6809	CAP_P_SMA-LF	alt_lio[10B2]
C6810	CAP_P_SMA-LF	alt_lio[10B2]
C6812	CAP_402	alt_lio[10B4]
C6813	CAP_402	alt_lio[10B3]
C6821	CAP_402	alt_lio[10C6]
C6822	CAP_603	alt_lio[10A4]
C6823	CAP_402	alt_lio[10A4]
C6825	CAP_402	alt_lio[10A3]
C6826	CAP_603	alt_lio[10D3]
C6830	CAP_402	alt_lio[10D4]
C6832	CAP_402	alt_lio[10B2]
C6833	CAP_402	alt_lio[10B2]
C6835	CAP_402	alt_lio[10D6]
C6836	CAP_402	alt_lio[10D3]
C7000	CAP_402	alt_lio[11C4]
C7010	CAP_805-1	alt_lio[11C5]
C7011	CAP_805-1	alt_lio[11C5]
C7012	CAP_805-1	alt_lio[11B5]
C7013	CAP_805-1	alt_lio[11B5]
C7014	CAP_805-1	alt_lio[11C3]
C7015	CAP_805-1	alt_lio[11B3]
C7100	CAP_402	alt_lio[12D5]
C7101	CAP_603	alt_lio[12D5]
C7102	CAP_P_B2	alt_lio[12D3]
C7104	CAP_402	alt_lio[12D4]
C7105	CAP_402	alt_lio[12D4]
C7110	CAP_603	alt_lio[12C4]
C7111	CAP_603	alt_lio[12C3]
C7112	CAP_402	alt_lio[12C4]
C7114	CAP_P_B2	alt_lio[12C3]
C7120	CAP_P_SMA-LF	alt_lio[12B6]
C7121	CAP_402	alt_lio[12B4]
C7122	CAP_0603	alt_lio[12B4]
C7130	CAP_P_SMA-LF	alt_lio[12A6]
C7131	CAP_402	alt_lio[12A4]
C7132	CAP_0603	alt_lio[12A4]
C7200	CAP_603	alt_lio[13B1]
C7201	CAP_P_CASE-C2-SM	alt_lio[13C2]
C7202	CAP_P_CASE-C2-SM	alt_lio[13C2]
C7203	CAP_P_CASE-C2-SM	alt_lio[13C1]
C7204	CAP_P_CASE-C2-SM	alt_lio[13C1]
C7210	CAP_402	alt_lio[13D7]
C7211	CAP_402	alt_lio[13D6]
C7212	CAP_603	alt_lio[13D5]
C7213	CAP_P_B2	alt_lio[13D5]
C7214	CAP_402	alt_lio[13D6]
C7220	CAP_402	alt_lio[13C7]
C7221	CAP_402	alt_lio[13C6]
C7222	CAP_603	alt_lio[13C5]
C7223	CAP_P_B2	alt_lio[13C5]
C7224	CAP_402	alt_lio[13C6]
C7230	CAP_402	alt_lio[13B7]
C7231	CAP_402	alt_lio[13B6]
C7232	CAP_603	alt_lio[13B5]
C7233	CAP_P_B2	alt_lio[13B5]
C7234	CAP_402	alt_lio[13B6]
C7240	CAP_402	alt_lio[13A7]
C7241	CAP_402	alt_lio[13A6]
C7242	CAP_603	alt_lio[13A5]
C7243	CAP_P_B2	alt_lio[13A5]
C7244	CAP_402	alt_lio[13A6]
C7260	CAP_402	alt_lio[13D3]
C7261	CAP_402	alt_lio[13D3]
C7270	CAP_402	alt_lio[13C3]
C7271	CAP_402	alt_lio[13C3]
C7280	CAP_402	alt_lio[13B3]
C7281	CAP_402	alt_lio[13B3]
C7290	CAP_402	alt_lio[13A3]
C7291	CAP_402	alt_lio[13A3]
C7300	CAP_402	alt_lio[14C7]
C7301	CAP_402	alt_lio[14C5]
C7302	CAP_402	alt_lio[14C5]
C7303	CAP_402	alt_lio[14C5]
C7304	CAP_402	alt_lio[14C5]
C7305	CAP_402	alt_lio[14C5]
C7350	CAP_402	alt_lio[14A7]
C7351	CAP_603	alt_lio[14A7]
C7352	CAP_402	alt_lio[14A5]
C7353	CAP_402	alt_lio[14A5]
C7354	CAP_402	alt_lio[14A5]
C7355	CAP_402	alt_lio[14A5]
C7356	CAP_402	alt_lio[14A5]
C7400	CAP_402	alt_lio[15B4]
C7401	CAP_402	alt_lio[15D7]
C7402	CAP_402	alt_lio[15C7]
C7404	CAP_402	alt_lio[15C4]
C7411	CAP_402	alt_lio[15B7]
C7412	CAP_402	alt_lio[15B6]
C7414	CAP_402	alt_lio[15C4]
C7442	CAP_402	alt_lio[15A3]
C7443	CAP_402	alt_lio[15A2]
C7445	CAP_402	alt_lio[15A2]
C7446	CAP_402	alt_lio[15A1]
C7447	CAP_402	alt_lio[15A1]
C7450	CAP_402	alt_lio[15A4]
C7451	CAP_402	alt_lio[15A5]
C7800	CAP_603	alt_lio[16C6]
C7801	CAP_603	alt_lio[16C6]
C7802	CAP_603	alt_lio[16C6]
C7806	CAP_402	alt_lio[16B8]
C7807	CAP_402	alt_lio[16B6]
C7808	CAP_402	alt_lio[16B7]
C7809	CAP_402	alt_lio[16C4]
C7822	CAP_402	alt_lio[16B4]
C7830	CAP_1210	alt_lio[16C3]
C7840	CAP_805	alt_lio[16B2]
C7841	CAP_P_SMC-LF	alt_lio[16B2]
C7842	CAP_805	alt_lio[16B2]
C7843	CAP_402	alt_lio[16B2]
C7890	CAP_402	alt_lio[16C1]
C8200	CAP_805	alt_lio[17D7]
C8201	CAP_805	alt_lio[17D7]
C8203	CAP_402	alt_lio[17D7]
C8204	CAP_603	alt_lio[17D6]
C8205	CAP_603	alt_lio[17D4]
C8206	CAP_402	alt_lio[17C2]
D5100	DIODE_SCHOT_3P_A_SC-75	alt_lio[5A3]
D5110	DIODE_SCHOT_3P_A_SC-75	alt_lio[5C4]
D6800	DIODE_SCHOT_POWERDI-123	alt_lio[10B4]
D7800	DIO_MBRM140T3_SM_SMD	alt_lio[16B3]
D8200	DIODE_SCHOT_3P_A_SC-75	alt_lio[17C7]
DZ7300	SUPPR_TRANSIENT_4P1_0405	alt_lio[14C6]
DZ7301	SUPPR_TRANSIENT_4P1_0405	alt_lio[14C6]
DZ7350	SUPPR_TRANSIENT_4P1_0405	alt_lio[14A6]
DZ7351	SUPPR_TRANSIENT_4P1_0405	alt_lio[14A6]
F8200	FUSE_1206	alt_lio[17D5]
FL5500	FILTER_4P_TCM1005	alt_lio[8C3]
FL5501	FILTER_4P_TCM1005	alt_lio[8B3]
J5100	CON_F4RT_USB_S2MT_TH_F-RT-TH-USB-LFT	alt_lio[5B2]
J5110	CON_F4RT_USB_S2MT_TH_F-RT-TH-USB-LFT	alt_lio[5C2]
J5300	CON_F26RT_S2MT_SM_F-RT-SM	alt_lio[6D2]
J5400	CON_F52RT_D2MT_SM_F-ST-SM	alt_lio[7C5]
J5500	CON_F80ST_D4MT_SM_F-ST-SM	alt_lio[8C4]
J7300	CON_F8RT_SPDIFTRAN_TH2_F-RT-TH	alt_lio[14D8]
J7350	CON_F8RT_SPDIFRCVR_TH2_F-RT-TH	alt_lio[14B8]
J7380	CON_M3ST_S_TH_M-ST-TH	alt_lio[14D1]
J7381	CON_M5ST_S_TH_M-ST-TH	alt_lio[14C1]
J7382	CON_M5ST_S_TH_M-ST-TH	alt_lio[14C1]
J8200	CON_F5RT_S2MT_TH3_F-RT-TH	alt_lio[17D8]
J8215	CON_M8RT_S_SM_M-RT-SM	alt_lio[18C5]
L5100	FILTER_4P_SM	alt_lio[5B4]
L5101	IND_SM	alt_lio[5B4]
L5110	FILTER_4P_SM	alt_lio[5C4]
L5111	IND_SM	alt_lio[5D4]
L5150	IND_SM	alt_lio[5A4]
L5160	IND_SM	alt_lio[5C4]
L6800	IND_0402	alt_lio[10A5]
L6801	IND_0402	alt_lio[10D6]
L6802	IND_0402	alt_lio[10D4]
L6803	IND_0402	alt_lio[10D3]
L7101	IND_0402	alt_lio[12D6]
L7102	IND_0402	alt_lio[12C6]
L7200	IND_0402	alt_lio[13B2]
L7201	IND_0402	alt_lio[13D7]
L7210	IND_0402	alt_lio[13D7]
L7220	IND_0402	alt_lio[13C7]
L7230	IND_0402	alt_lio[13B7]
L7240	IND_0402	alt_lio[13A7]
L7300	IND_0603	alt_lio[14D6]
L7301	IND_0603	alt_lio[14D4]
L7302	IND_0402	alt_lio[14D6]
L7303	IND_0402	alt_lio[14C6]
L7304	IND_0402	alt_lio[14C4]
L7305	IND_0402	alt_lio[14C6]
L7306	IND_0402	alt_lio[14C4]
L7307	IND_0402	alt_lio[14C6]
L7350	IND_0402	alt_lio[14B6]
L7351	IND_0402	alt_lio[14B4]
L7352	IND_0402	alt_lio[14B6]
L7353	IND_0402	alt_lio[14B6]
L7354	IND_0402	alt_lio[14B4]
L7355	IND_0402	alt_lio[14B6]
L7356	IND_0402	alt_lio[14B4]
L7357	IND_0402	alt_lio[14A6]
L7400	IND_0402	alt_lio[15B4]
L7800	IND_IHLP	alt_lio[16B3]
L8200	FILTER_4P_SM	alt_lio[17D6]
L8201	IND_SM-1	alt_lio[17D6]
PD6401	PHOTODIODE_2P_TH	alt_lio[9C6]
Q5101	TRA_2N7002_SOT23-LF	alt_lio[5C7]
Q5360	TRA_2N7002_SOT23-LF	alt_lio[6B3]
Q6401	TRA_2N7002_SOT23-LF	alt_lio[9C5]
Q7400	TRA_2N7002DW_SOT-363	alt_lio[15D7 15C7]
Q7401	TRA_2N7002DW_SOT-363	alt_lio[15D6 15D5]
Q7402	TRA_2N7002DW_SOT-363	alt_lio[15B7 15C5]
Q7403	TRA_2N7002DW_SOT-363	alt_lio[15A8 15A7]
Q7800	TRA_FDM6296_MICROFET 3X3	alt_lio[16C4]
Q7801	TRA_FDM6296_MICROFET 3X3	alt_lio[16B4]
Q7890	TRA_FDC638P_SM-LF	alt_lio[16C2]
Q8200	TRA_2N7002DW_SOT-363	alt_lio[17C3 17C1]
Q8201	TRA_2N7002DW_SOT-363	alt_lio[17C1 17C2]
Q8209	TRA_TP0610_S0T23-3	alt_lio[17D2]
R0600	RES_402	alt_lio[4A4]
R0601	RES_402	alt_lio[4A3]
R5101	RES_402	alt_lio[5D7]
R5102	RES_402	alt_lio[5C7]
R5300	RES_402	alt_lio[6C6]
R5301	RES_402	alt_lio[6C6]
R5352	RES_402	alt_lio[6A6]
R5353	RES_402	alt_lio[6B5]
R5354	RES_402	alt_lio[6B5]
R5360	RES_402	alt_lio[6B3]
R5361	RES_402	alt_lio[6B3]
R5500	RES_402	alt_lio[8B4]
R6401	RES_402	alt_lio[9C6]
R6402	RES_402	alt_lio[9C6]
R6403	RES_402	alt_lio[9C5]
R6404	RES_402	alt_lio[9C5]
R6405	RES_402	alt_lio[9C5]
R6406	RES_402	alt_lio[9C4]
R6407	RES_402	alt_lio[9C4]
R6800	RES_402	alt_lio[10C6]
R6802	RES_402	alt_lio[10A5]
R6803	RES_402	alt_lio[10A5]
R6807	RES_402	alt_lio[10C7]
R6808	RES_402	alt_lio[10D3]
R6810	RES_402	alt_lio[10A3]
R6811	RES_402	alt_lio[10A3]
R6852	RES_402	alt_lio[10B8]
R6853	RES_402	alt_lio[10B8]
R7000	RES_402	alt_lio[11B3]
R7001	RES_402	alt_lio[11B6]
R7002	RES_402	alt_lio[11C5]
R7003	RES_402	alt_lio[11B5]
R7010	RES_402	alt_lio[11C4]
R7011	RES_402	alt_lio[11C4]
R7012	RES_402	alt_lio[11C4]
R7013	RES_402	alt_lio[11C4]
R7014	RES_402	alt_lio[11B4]
R7015	RES_402	alt_lio[11B4]
R7016	RES_402	alt_lio[11B4]
R7017	RES_402	alt_lio[11B4]
R7100	RES_402	alt_lio[12C5]
R7101	RES_603	alt_lio[12D4]
R7110	RES_402	alt_lio[12C3]
R7111	RES_402	alt_lio[12C3]
R7112	RES_603	alt_lio[12D3]
R7113	RES_603	alt_lio[12C2]
R7120	RES_402	alt_lio[12B5]
R7121	RES_402	alt_lio[12B4]
R7122	RES_402	alt_lio[12B4]
R7123	RES_402	alt_lio[12B4]
R7124	RES_402	alt_lio[12B4]
R7130	RES_402	alt_lio[12A5]
R7131	RES_402	alt_lio[12A4]
R7132	RES_402	alt_lio[12A4]
R7133	RES_402	alt_lio[12A4]
R7134	RES_402	alt_lio[12A4]
R7201	RES_402	alt_lio[13D6]
R7202	RES_402	alt_lio[13D5]
R7203	RES_402	alt_lio[13C5]
R7204	RES_402	alt_lio[13B5]
R7260	RES_402	alt_lio[13D4]
R7261	RES_402	alt_lio[13D4]
R7270	RES_402	alt_lio[13C4]
R7271	RES_402	alt_lio[13C4]
R7280	RES_402	alt_lio[13B4]
R7281	RES_402	alt_lio[13B4]
R7290	RES_402	alt_lio[13A4]
R7291	RES_402	alt_lio[13A4]
R7300	RES_402	alt_lio[14C4]
R7301	RES_402	alt_lio[14C4]
R7320	RES_402	alt_lio[14D7]
R7321	RES_402	alt_lio[14B7]
R7323	RES_402	alt_lio[14B6]
R7349	RES_402	alt_lio[14B7]
R7350	RES_402	alt_lio[14A4]
R7351	RES_402	alt_lio[14A4]
R7380	RES_402	alt_lio[14C2]
R7381	RES_402	alt_lio[14C1]
R7390	RES_402	alt_lio[14B2]
R7401	RES_402	alt_lio[15D8]
R7402	RES_402	alt_lio[15D7]
R7403	RES_402	alt_lio[15C7]
R7404	RES_402	alt_lio[15C4]
R7405	RES_402	alt_lio[15D5]
R7406	RES_402	alt_lio[15D6]
R7411	RES_402	alt_lio[15C8]
R7412	RES_402	alt_lio[15B7]
R7413	RES_402	alt_lio[15C6]
R7414	RES_402	alt_lio[15C4]
R7415	RES_402	alt_lio[15C5]
R7416	RES_402	alt_lio[15C6]
R7417	RES_402	alt_lio[15A8]
R7418	RES_402	alt_lio[15A7]
R7450	RES_402	alt_lio[15A5]
R7451	RES_402	alt_lio[15A5]
R7452	RES_402	alt_lio[15A5]
R7453	RES_402	alt_lio[15A4]
R7454	RES_402	alt_lio[15A4]
R7460	RES_402	alt_lio[15C7]
R7800	RES_402	alt_lio[16B2]
R7802	RES_402	alt_lio[16C6]
R7804	RES_402	alt_lio[16C7]
R7805	RES_402	alt_lio[16B7]
R7806	RES_402	alt_lio[16B8]
R7808	RES_402	alt_lio[16B7]
R7810	RES_402	alt_lio[16B4]
R7821	RES_402	alt_lio[16B3]
R7822	RES_402	alt_lio[16B3]
R7823	RES_402	alt_lio[16C5]
R7830	RES_402	alt_lio[16C6]
R7890	RES_402	alt_lio[16C2]
R8200	RES_402	alt_lio[17C2]
R8201	RES_402	alt_lio[17D2]
R8202	RES_402	alt_lio[17D5]
R8203	RES_402	alt_lio[17C5]
R8204	RES_402	alt_lio[17C6]
R8205	RES_402	alt_lio[17D3]
R8208	RES_402	alt_lio[17D5]
R8209	RES_402	alt_lio[17D1]
R8210	RES_402	alt_lio[17D1]
R8211	RES_402	alt_lio[17C2]
R8290	RES_402	alt_lio[17C5]
R8291	RES_402	alt_lio[17C4]
U5100	SWI_TPS2042B_MSOP	alt_lio[5B6]
U5300	PWR_CNTRL_TPS2231_QFN	alt_lio[6C5]
U5351	MC74VHC1G00_SC70-5	alt_lio[6A6]
U5352	MC74VHC1G08_SC70	alt_lio[6A5]
U5360	MC74VHC1G00_SC70-5	alt_lio[6B2]
U6401	OPAMP_MAX4236EUTT_SOT23-6-LF	alt_lio[9C5]
U6800	AUDIO_STAC9220_LQFP	alt_lio[10D5]
U7000	OPAMP_MAX4253_UMAX	alt_lio[11B4 11C4]
U7100	MAX9722_QFN	alt_lio[12D4]
U7210	MAX9705_TDFN	alt_lio[13D6]
U7220	MAX9705_TDFN	alt_lio[13C6]
U7230	MAX9705_TDFN	alt_lio[13B6]
U7240	MAX9705_TDFN	alt_lio[13A6]
U7800	ISL6269_QFN	alt_lio[16C6]
U8290	COMPARATOR_LM397_SOT23-5	alt_lio[17C4]
VR6800	LREG_TPS79501_SOT223-6	alt_lio[10A4]
VR8290	SHNTREG_LM431_SOT23-3-LF	alt_lio[17C5]
XW6800	SHORT_SM	alt_lio[10A8]
XW6801	SHORT_SM	alt_lio[10B5]
XW7100	SHORT_SM	alt_lio[12C5]
XW7101	SHORT_SM	alt_lio[12C5]
XW7103	SHORT_SM	alt_lio[12C4]
XW7200	SHORT_SM	alt_lio[13B6]
XW7310	SHORT_SM	alt_lio[14B2]
XW7311	SHORT_SM	alt_lio[14B2]
XW7312	SHORT_SM	alt_lio[14B2]
XW7400	SHORT_SM	alt_lio[15A4]
XW7800	SHORT_SM	alt_lio[16B6]

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